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Study of MoS_2 and graphene-based heterojunctions for electronic and sensing applications

by

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Dedication

To my parents, Sayeda Sultana and Sikder Jahangir Rashid

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Acknowledgements

I would like to thank my Supervisor Dr. MVS Chandrashekhar for supporting me during these three years. Working with Dr. Chandra, in my opinion, is the best thing that a Ph.D student can wish for. He perfectly translates the character of his students and provides the best conditions for the development of intellectual qualities and creative thinking. I am very grateful to him for his scientific advice and knowledge and many insightful discussions and suggestions he provided me and beyond all his guidance in my tough times.

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I wish to express my heartfelt gratitude to my family – my parents and my brother, for always having faith in me and for bringing me this far. I would also like to thank all my friends who were very supportive during the entire duration of my stay here in Columbia, South Carolina. Finally and most importantly, I would like to express my deep gratitude towoards the Almighty for giving me the ability to finish this work smoothly, I could not have achieved anything without His blessings.

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Abstract

Since the discovery of graphene, there has been an increase in two-dimensional (2D) materials research for their scalability down to atomic dimensions. Among the analogs of graphene, transition metal dichalcogenides (TMDs) are attractive due to their exceptional electronic and optoelectronic properties. MoS_2, a TMD, has several advantages over graphene and the industry workhorse Si, and has been reported to demonstrate excellent transistor performances. The key obstacle in the commercialization of MoS_2 technology is low carrier mobility over large areas for top-down devices. Although there were several early reports on synthesis of atomically thin MoS_2 with moderate mobility, transferring large area grown films to a substrate of choice leads to interface charges that degrade mobility. In our work, a top-down growth technique for synthesizing large area, 3-5 monolayers (ML) thick MoS_2 film have been presented by pre-oxidation of metallic Mo instead of direct sulfidation. The growth temperature was significantly reduced in this method, eliminating free sulfur-induced degradation of the SiO_2 gate dielectric. As a result, the leakage current was suppressed by a factor of $>10^8$, when compared to a single step direct sulfidation method. Using these thin films, back-gated field effect transistors have been demonstrated with accumulation electron mobility >80 cm^2/Vs, on/off $>10^5$, and subthreshold swing of 84 mV/dec; which are among the best results for MoS_2 based transistors on SiO_2 substrate. A hypothesis on current saturation has also been presented, attributing it to charge control rather than velocity saturation.

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The second part of our work aims at utilizing the best properties both graphene and MoS_2 simultaneously by forming a heterojunction of these two atomically thin materials. Interestingly, these two materials have certain contrasting properties, for example, graphene based FETs have poor switching performance while MoS_2 based FETs can outperform many state-of-the-art ultra-low power transistors. Fabricating a Schottky diode made of graphene and MoS_2 allows the unique properties of these two materials to be combined and has been shown to be useful. A key property of these 2D heterojunctions is that each constituent of the heterojunction is so thin that it may not be able to completely screen an electric field from the second constituent, i.e. the Debye screening length can be greater than the layer thicknesses, so that voltage-induced interfacial tuning is achievable. This capability is unique to thin layers, most practically achieved in 2D heterojunctions, and has been exploited in recent “barristors”, which are 3-terminal devices with Schottky diodes where the barrier height can be tuned by an insulated gate. Such a tunable Schottky diode, similar to a triode vacuum tube is attractive for applications in RF circuits, photodetection and chemical sensing, analog and digital electronics, etc, with all the advantages of solid state devices e.g. high speed, low-cost and compactness. In this work, a graphene/MoS_2 heterojunction on SiO_2 dielectric has been fabricated to demonstrate a functional barristor device. By varying the gate bias between -20 V and +10 V, the barrier height could be modulated by >0.65 eV, potentially enabling current control over 10 orders of magnitude at room temperature. Using the current-voltage (I-V) and capacitance-voltage (C-V) characteristics of this device, we have also extracted the Richardson’s coefficient and electronic effective mass in MoS_2 using a thermionic emission model, which are very important parameters

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required for proper engineering of these devices. After that, various applications of the barristor device have also been explored. The high optical response of the barristor has demonstrated the presence of photoconductive gain, and has been consistent with the changes in Schottky barrier height caused by the back-gate. The barristor has also been successful as gate-tunable toxic gas sensors, with lowest level detection lying around 100 ppb (parts per billion) for NO_2 and 1 ppm (parts per million) for NH_3. These observations highlight the potential applications of the graphene/MoS_2 barristor for various electronic, optoelectronic and sensing applications.

Finally, a mixed dimensional barristor made of graphene/InN nanowire heterojunction with a backgate has been demonstrated. The surface passivation of InN and the tunnel barrier formation at the graphene/NW interface have been achieved through controlled O_2 plasma exposure, which has allowed an otherwise ohmic contact to turn into a gate tunable Schottky junction with >1 eV barrier height. This device has been demostrated to perform sub-ppb level trace gas detection, photo-detection with very high sensitivity and a novel gate-controllable memristive action through longer O_2 plasma exposure.

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Chapter 1

Introduction

1.1 Overview

Since the discovery of graphene, there has been an increase in two-dimensional (2D) materials research for their scalability down to atomic dimensions.[1],[2] Many other 2D materials are known, such as the TMDs or TMDCs,[3],[4], transition metal oxides including titania- and perovskite-based oxides,[5],[6] and graphene analogues such as boron nitride (BN).[7],[8] To be specific, TMDs exhibit a broad range of electronic, optical, mechanical, chemical and thermal properties that have been subjected to a great deal of scintific studies for decades.[4],[9],[10] However, the recent scientific and engineering interests are focused towards the atomically thin two dimensional forms of the TMDs because of the rapid advances in synthesis and fabrication, optical detection, transfer and manipulation of 2D materials, and better physical understanding of 2D materials resulting from a decade long study of graphene. The 2D exfoliated versions of TMDs offer properties that are complementary to graphene while being distinct in manner. Graphene displays an exceptionally high carrier mobility exceeding 10^6 $cm^2V^{-1}s^{-1}$ at 2 K (ref. 11) and exceeding 10^5 $cm^2V^{-1}s^{-1}$ at room temperature for devices encapsulated in BN dielectric layers.[12] Since pristine graphene suffers from the lack of a bandgap, field effect transistors (FETs) made from graphene (GFET) cannot be effectively switched off and therefore have very low on/off switching ratios. While it is possible to engineer

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bandgaps in graphene using nanostructuring,[13]-[15] chemical functionalization[16] and applying a high electric field to bilayer graphene,[17] unfortunately these methods add complexity to the manufacturing process and significantly diminish the mobility. In contrast, several 2D TMDs possess satisfactory bandgaps of around 1–2 eV, which is promising for interesting new FET and optoelectronic devices.

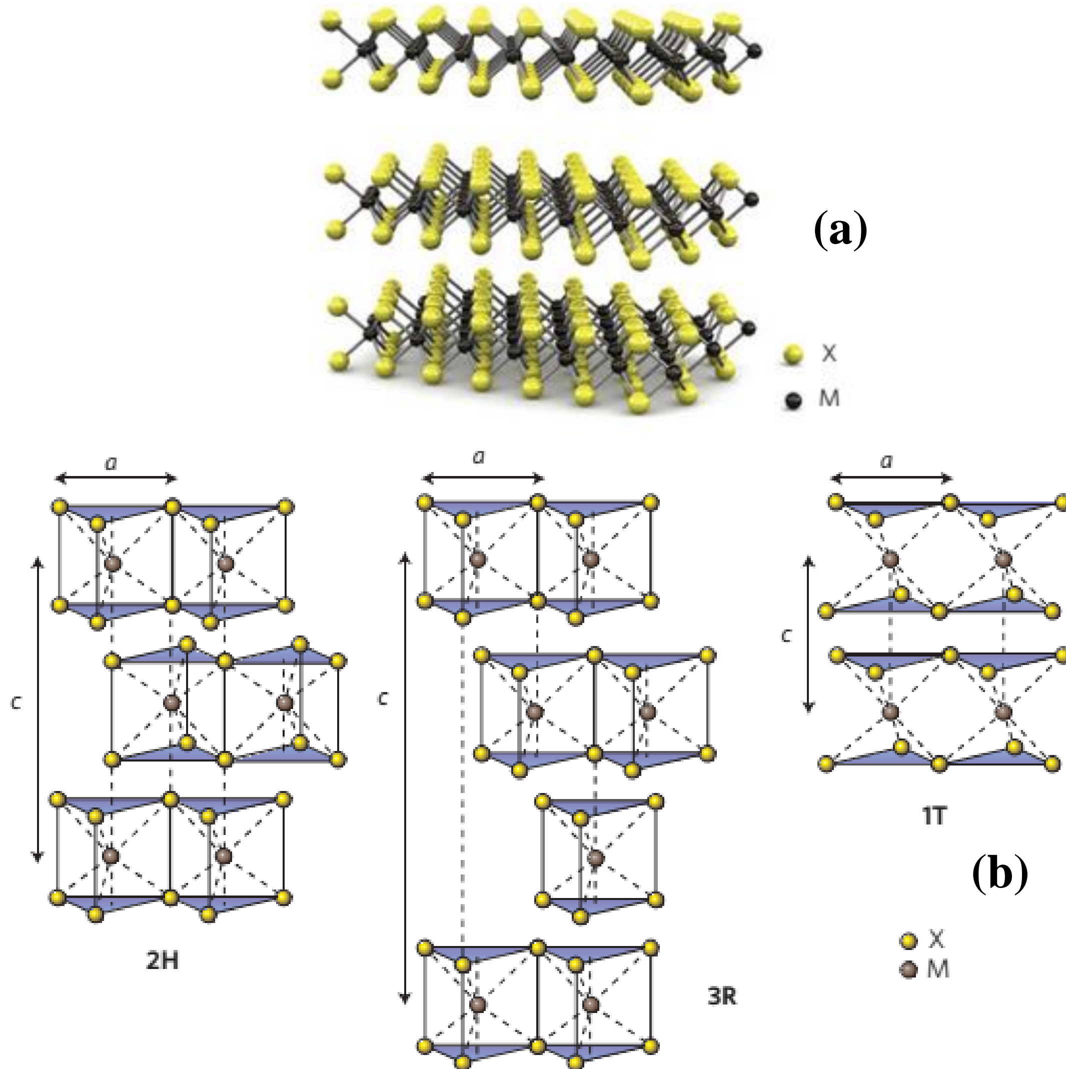

Figure 1.1: (a) Three-dimensional schematic representation of a typical MX_2 structure, with the chalcogen atoms (X) in yellow and the metal atoms (M) in grey.[18] (b) Schematics of the structural polytypes: 2H (hexagonal symmetry), 3R (rhombohedral symmetry, trigonal prismatic coordination) and 1T (tetragonal symmetry, octahedral coordination).[19]

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When a 2D material is combined with graphene to form a heterojunction, the Schottky barrier device possesses unique properties that cannot be found in bulk heterjunctions. For instance, since both materials are atomically thin, any electric field arising from an applied bias or from optical or chemical perturbation cannot be screened out completely by one material, and therefore affects both simultaneously. This may result in a batter control of the Schottky barrier height as both sides of the junction can be modulated at once, which can lead to highly sensitive photodetectors of chemidiodes. Introduction of a top or bottom gate allows more felxibility in the device design as the barrier height can then be modulated to fine tune the performance of the device. A device of such unique features is highly sought after, and is generally called a *barristor* (Schottky barrier transistor). In this work, we will start our discussion with TMDs, and then gradually shift towards the novel applications of the barristors made from them. The literature review provided in this chapter is adopted from ref. [20].

Table 1.1 Summary of TMD materials and properties.[20]

	$-S_2$	$-Se_2$	$-Te_2$
	Electronic characteristics	**Electronic characteristics**	**Electronic characteristics**
Nb	Metal; superconducting; CDW	Metal; superconducting; CDW	Metal
Ta	Metal; superconducting; CDW	Metal; superconducting; CDW	Metal
Mo	Semiconducting 1L: 1.8 eV Bulk: 1.2 eV	Semiconducting 1L: 1.5 eV Bulk: 1.1 eV	Semiconducting 1L: 1.1 eV Bulk: 1.0 eV
W	Semiconducting 1L: 2.1 eV 1L: 1.9 eV Bulk: 1.4 eV	Semiconducting 1L: 1.7 eV Bulk: 1.2 eV	Semiconducting 1L: 1.1 eV

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TMDs are a class of materials with the formula MX_2, where M is a transition metal element from group IV (Ti, Zr, Hf and so on), group V (for instance V, Nb or Ta) or group VI (Mo, W and so on), and X is a chalcogen (S, Se or Te). These materials form layered structures of the form X–M–X, with the chalcogen atoms in two hexagonal planes separated by a plane of metal atoms, as shown in Figure 1.1(a). Adjacent layers are weakly held together to form the bulk crystal in a variety of polytypes, which vary in stacking orders and metal atom coordination, as shown in Figure 1.1(b). The overall symmetry of TMDs is hexagonal or rhombohedral, and the metal atoms have octahedral or trigonal prismatic coordination. The electronic properties of TMDs range from metallic to semiconducting, as summarized in Table 1.1.[20]

TMDs are a class of materials with the formula MX_2, where M is a transition metal element from group IV (Ti, Zr, Hf and so on), group V (for instance V, Nb or Ta) or group VI (Mo, W and so on), and X is a chalcogen (S, Se or Te). These materials form layered structures of the form X–M–X, with the chalcogen atoms in two hexagonal planes separated by a plane of metal atoms, as shown in Figure 1.1(a). Adjacent layers are weakly held together to form the bulk crystal in a variety of polytypes, which vary in stacking orders and metal atom coordination, as shown in Figure 1.1(b). The overall symmetry of TMDs is hexagonal or rhombohedral, and the metal atoms have octahedral or trigonal prismatic coordination. The electronic properties of TMDs range from metallic to semiconducting, as summarized in Table 1.1.[20]

The relatively high earth abundance of TMDs and their direct bandgaps in the visible range make them attractive as the light-absorbing material in alternative thin-film solar cells,[20] including flexible photovoltaics that could coat buildings and curved

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structures.

1.2 Synthesis of MoS_2 and other 2D Materials

Atomically thin flakes of TMDCs can be peeled from their parent bulk crystals by micromechanical cleavage using adhesive tape[32-39], applied to substrates and optically identifid by light interference[40-41], using the same techniques that were developed for graphene. This method is not scalable, however, and does not allow systematic control of flake thickness and size. Recently, a focused laser spot has been used to thin MoS_2 down to monolayer thickness by thermal ablation with micrometre-scale resolution, but the requirement for laser raster scanning makes it challenging for scale-up[42].

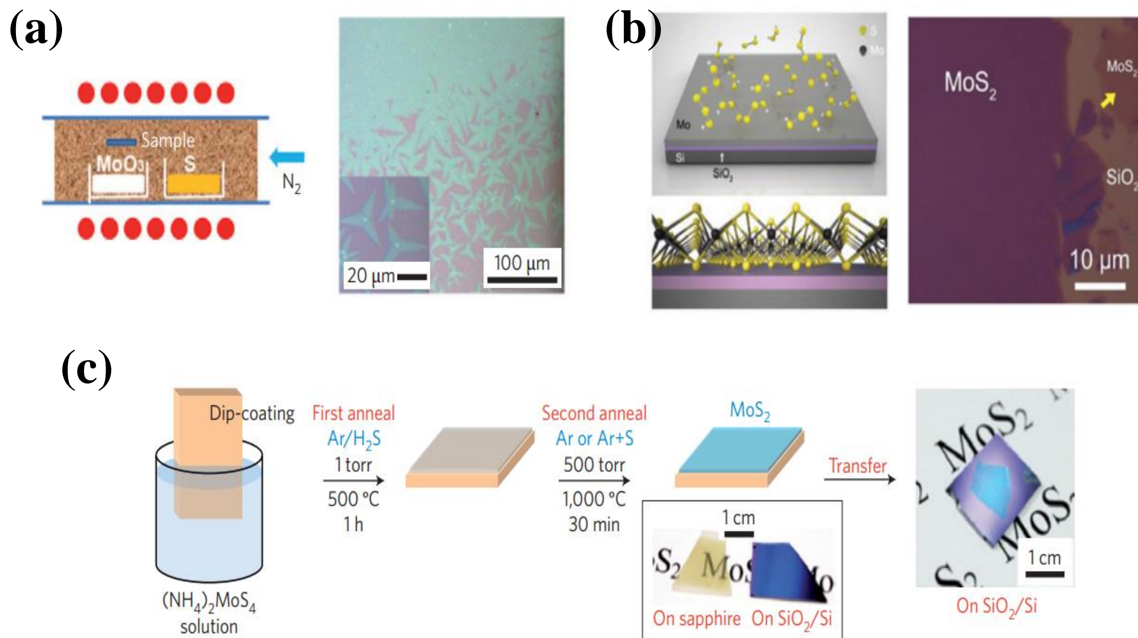

Figure 1.2: (a) Schematic of CVD of MoS_2 from solid S and MoO_3 precursors (left) and resulting MoS_2 films on SiO2 (right)[54]. The red dots indicate the heating elements in the furnace. In this optical microscopy image, the lighter regions are MoS_2 and the darker regions are SiO_2. (b) CVD growth of MoS_2 from a solid layer of Mo on SiO_2 exposed to S vapour (top left), resulting in MoS_2 layers that are visible in optical microscopy (right)[55]. Bottom left: side-view schematic of an MoS_2 layer on the Si/SiO_2 substrate. **(c)** CVD growth of MoS_2 from a dip-coated precursor on the substrate and growth in the presence of Ar gas and S vapour[56].

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For obtaining large quantities of exfoliated nanosheets, liquidphase preparations of TMDCs are very promising. The intercalation of TMDCs by ionic species[43-48] allows the layers to be exfoliated in liquid. The intercalation method was first demonstrated in the 1970s[48] and the subsequent exfoliation into thin layers by Morrison, Frindt and co-workers in the 1980s[45], and these methods are experiencing renewed interest today[46,47]. The typical procedure involves submerging bulk TMDC powder in a solution of a lithium-containing compound such as n-butyllithium for more than a day to allow lithium ions to intercalate, followed by exposing the intercalated material to water. The water reacts vigorously with the lithium between the layers to evolve H_2 gas, which rapidly separates the layers[44,46]. An alternative method of lithiation that is faster and more controllable uses an electrochemical cell with a lithium foil anode and TMDC-containing cathode, as recently demonstrated by Zeng *et al.*[47,49]. Because the intercalation occurs while a galvanic discharge is occurring in the electrochemical cell, the degree of lithiation can be monitored and controlled. The resulting Li-intercalated material is exfoliated by sonication in water as before, yielding monolayer TMDC nanosheets. Alternatively, TMDCs can be exfoliated by ultrasonication in appropriate liquids, including organic solvents, aqueous surfactant solutions, or solutions of polymers in solvents[50,51,52,53]. Typically, ultrasonication results in the mechanical exfoliation of layered crystals to give flakes that are a few hundred nanometres in size. The exfoliated nanosheets are stabilized against re-aggregation either by solvation or by steric or electrostatic repulsion due to the adsorption of molecules from solution.

Some CVD methods for growing atomically thin fims of MoS_2 on insulating substrates have recently been reported[54-56]. These methods use diffrent solid precursors

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heated to high temperatures: sulphur powder and MoO_3 powder vaporized and co deposited onto a nearby substrate[54,57]; a thin layer of Mo metal deposited onto a wafer heated with solid sulphur[55]; and substrates dip-coated in a solution of $(NH_4)_2MoS_4$ and heated in the presence of sulphur gas[56]. These CVD-related methods are summarized in Figure 1.2. In many of these methods, the final MoS_2 film thickness is dependent on the concentration or thickness of the initial precursor, although precise control of the number of layers over a large area has not yet been achieved. CVD growth of MoS_2 has also been demonstrated using previously CVD-grown graphene on Cu foil as a surface template, resulting in single-crystal flkes of MoS_2 several micrometres in lateral size75. These CVD reports are still relatively early results but hold promise that further work will lead to growth of materials other than MoS_2, and production of uniform, large-area sheets of TMDCs with controllable layer number.

1.3 Electronic Properties and Applications of the TMDs

Many TMDCs have band structures that are similar in their general features, as shown by first principles and tight-binding approximations and measured using a variety of spectroscopic tools[58-63]. In general, MoX_2 and WX_2 compounds are semiconducting whereas NbX_2 and TaX_2 are metallic[58-63]. The band structures of bulk and monolayer MoS_2 calculated from first principles are shown in Figure 1.3[68]. At the Γ-point, the bandgap transition is indirect for the bulk material, but gradually shifts to be direct for the monolayer[56,57,69-71]. The direct excitonic transitions at the K-point remain relatively unchanged with layer number[36].

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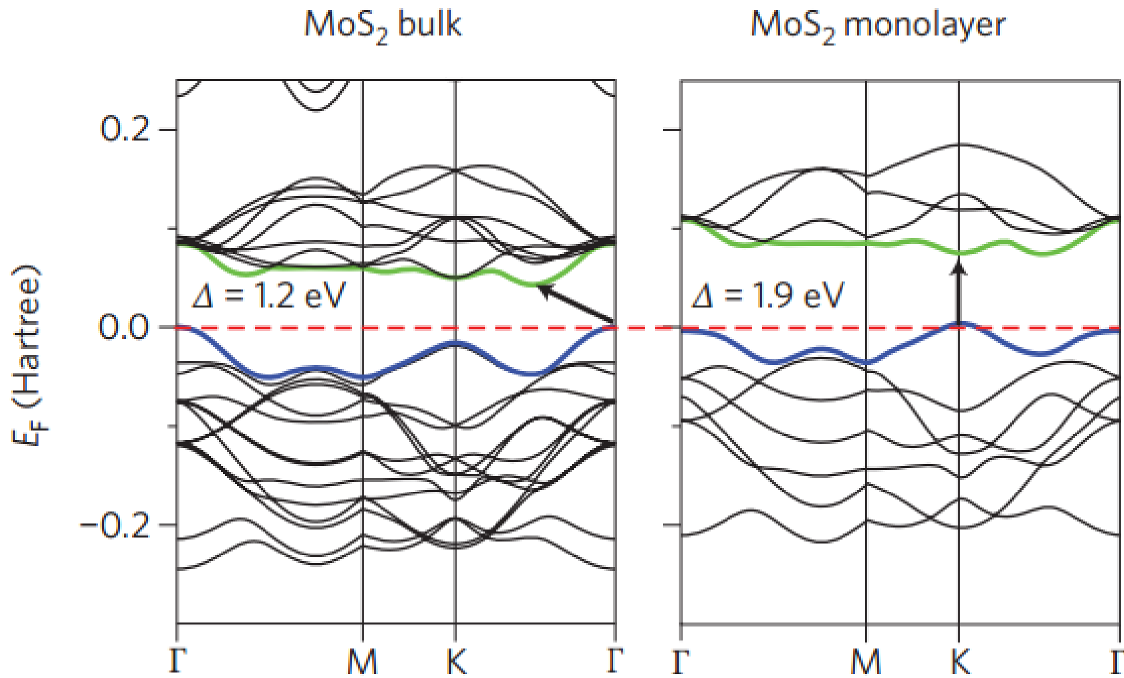

Figure 1.3: Band structures calculated from first-principles density functional theory (DFT) for bulk (left) and monolayer (right) MoS_2.

The change in the band structure with layer number is due to quantum confinement and the resulting change in hybridization between p_z orbitals on S atoms and *d* orbitals on Mo atoms[59,72,73]. The electronic distributions are also spatially correlated to the atomic structure[73]. For MoS_2, density functional theory (DFT) calculations show that the conduction-band states at the K-point are mainly due to localized *d* orbitals on the Mo atoms, located in the middle of the S–Mo–S layer sandwiches and relatively unaffected by interlayer coupling. However, the states near the Γ-point are due to combinations of the antibonding p_z-orbitals on the S atoms and the *d* orbitals on Mo atoms, and have a strong interlayer coupling effect[73]. Therefore, as the layer numbers change, the direct excitonic states near the K-point are relatively unchanged, but the transition at the Γ-point shift significantly from an indirect one to a larger, direct one. All MoX_2 and WX_2 compounds are expected to undergo a similar indirect- to direct-bandgap transformation

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with decreasing layer numbers, covering the bandgap energy range 1.1–1.9 eV[58-67]. The bulk and monolayer bandgaps for several TMDCs are summarized in Table 1.1.

The bandgap in most semiconducting TMDCs, whether in bulk or monolayer, are comparable to the 1.1-eV bandgap in silicon, as listed in Table 1.1, making them suitable for use as digital transistors[74]. The electronic band structure also determines photophysical properties.

One of the most important applications of semiconductors is for transistors in digital electronics. In the past few decades, progress in the digital electronics industry has been driven by scaling transistors to ever-smaller dimensions. Currently, state-of-the-art processors have silicon-based metal–oxide–semiconductor field-effect transistors (MOSFETs) with feature lengths of 22 nm[75]. Subsequent reductions in scale will soon approach limits due to statistical and quantum effects and difficulty with heat dissipation[75], motivating the search for new device concepts and materials. In particular, 2D semiconductor materials are attractive for processability and lack of short-channel effects that can hinder device performance[74].

In the basic FET structure, which has been adapted to 2D TMDCs[38,77], a semiconducting channel region is connected to the source and drain electrodes, and separated by a dielectric layer from a gate electrode[76]. The current flowing between the source and drain electrodes is controlled by the gate electrode modulating the conductivity of the channel. Silicon is the primary material that meets the industrial requirements for performance and manufacturability in digital logic for computing, although other semiconductors such as SiC, GaN, Ge and GaAs have more specialized applications such as light-emitting diodes (LEDs), high-power electronics, high-

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temperature electronics, radiofrequency electronics and photovoltaics[78]. Other nanomaterials that are being explored and evaluated include carbon nanotubes[79-80], graphene [79,82,82] and semiconductor nanowires[81].

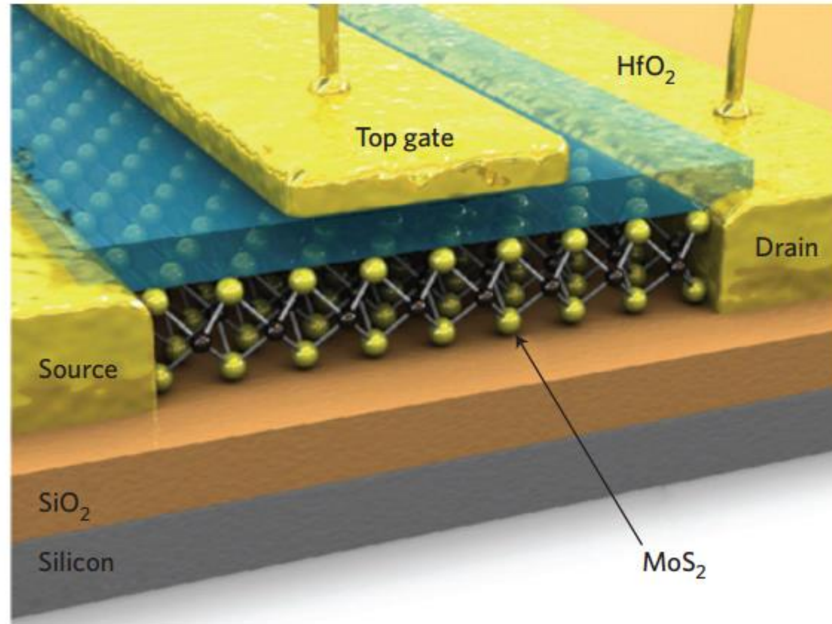

Figure 1.4: Schematic illustration of HfO_2-top-gated monolayer MoS_2 FET device [38].

For digital logic transistors, desirable properties are high charge-carrier mobilities for fast operation, a high on/off ratio (that is, the ratio of on-state to off-state conductance) for effective switching, and high conductivity (that is, the product of charge density and mobility) and low off-state conductance for low power consumption during operation. In most semiconductors, doping can be used to increase the charge density, but can also lead to decreased mobility owing to scattering[75,81]. For digital logic, on/off ratios of 10^4–10^7 are generally required for use as switches [74,79]. Much interest in graphene has centred on electronic device applications because it is two-dimensional, it has exceptionally high carrier mobilities, and an external gate voltage can readily modulate its current flow[74]. Graphene has been used in high-frequency radiofrequency analog transistors with cut-off

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frequencies reaching hundreds of gigahertz, taking advantage of the high carrier mobilities and high transconductances[74,82,83]. But the lack of bandgap in graphene means that it cannot achieve a low off-state current, limiting its use as a digital logic transistor. There is a clear need for new nanoelectronic materials with a sizable bandgap to support high on/off ratios while maintaining high carrier mobilities and scalability to ever-smaller dimensions.

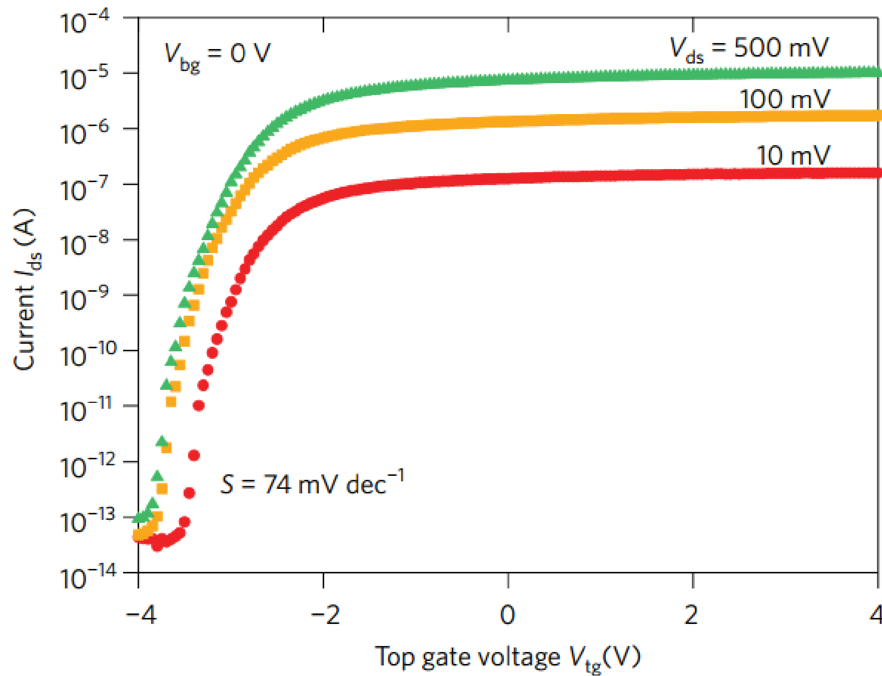

Figure 1.5: Source–drain current (I_{ds}) versus top gate voltage (V_{tg}) curve recorded from the top-gated device in Figure 5.1 for a bias voltage ranging from 10 mV to 500 mV[38]. Measurements are performed at room temperature with the back gate grounded. Top gate width, 4 mm; top gate length, 500 nm. The device can be completely turned off by changing the top gate bias from −2 to −4 V. For V_{ds} = 10 mV, the I_{on}/I_{off} ratio is >1 × 10^6. For V_{ds} = 500 mV, the I_{on}/I_{off} ratio is >1 × 10^8 in the measured range while the subthreshold swing S = 74 mV dec^{-1}.

Flexibility and transparency are also desirable characteristics for next-generation electronics. Researchers are now turning to TMDCs as ultrathin materials with tunable bandgaps that can be made into FETs with high on/off ratios[38,84]. Two-dimensional semiconductors such as MoS_2 and others offer an important advantage when compared

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with classical 3D electronic materials: their subnanometre thickness. Coupled with a bandgap typically in the 1–2-eV range which can result in high on/off ratios, their extreme thinness allows more efficient control over switching[85] and can help to reduce short-channel effects and power dissipation, the main limiting factors to transistor miniaturization.

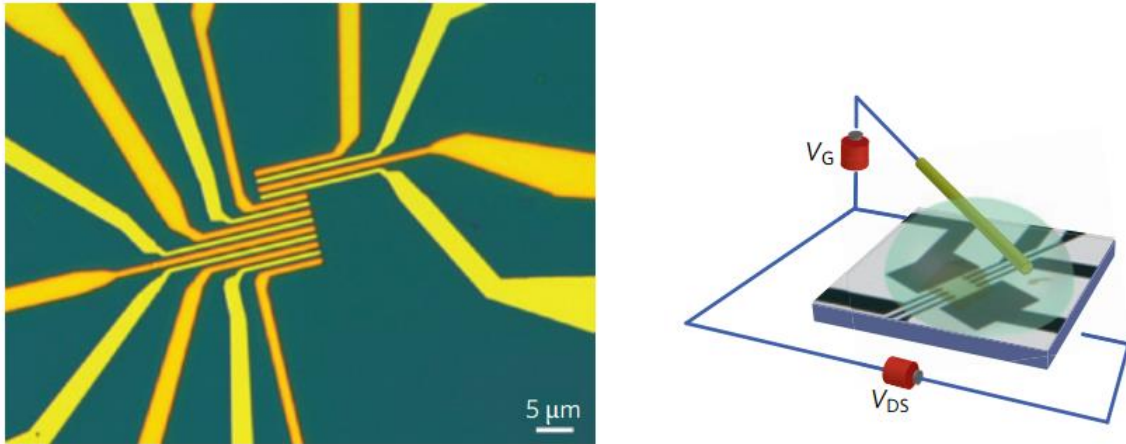

Figure 1.6: (Left) Integrated circuit based on single-layer MoS_2[84]. (Right) Schematic of electric double-layer transistor (EDLT, a FET gated by ionic liquids)[86]. V_{DS} is the source–drain voltage and V_G is the gate voltage.

Semiconducting 2D TMDCs have unique features that make them attractive as a channel material in FETs such as the lack of dangling bonds, structural stability and mobility comparable to Si [89]. One of the earliest uses of TMDCs in FETs was reported in 2004, where WSe_2 crystals showed mobility comparable to the best single-crystal Si FETs (up to 500 $cm^2\ V^{-1}\ s^{-1}$ for p-type conductivity at room temperature), ambipolar behaviour and a 10^4 on/off ratio at a temperature of 60 K[90]. This result was soon followed by devices based on thin layers of MoS_2 with a back-gated configuration, resulting in mobility values in the range 0.1–10 $cm^2\ V^{-1}\ s^{-1}$ [32,77].

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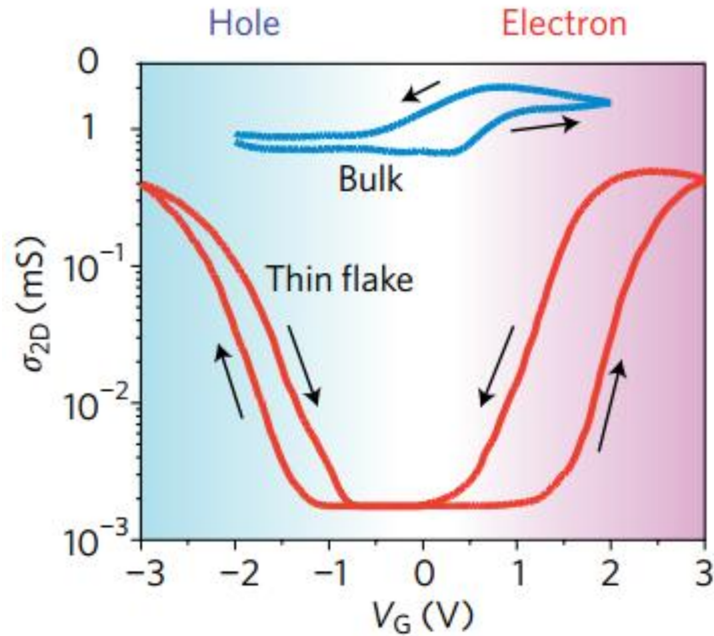

Figure 1.7: Conductivity as a function of top gate voltage for both bulk and thin-flake MoS_2 EDLT devices[86]. Thin-flake devices show on/off ratios $>10^2$ for both electron and hole transport.

The first implementation of a top-gated transistor based on monolayer MoS_2 was reported by Kis and co-workers[38], as shown in Figure 1.4. This device showed excellent on/off current ratio (~10^8), n-type conduction, room-temperature mobility of >200 cm^2 V^{-1} s^{-1} and subthreshold swing of 74 mV per decade[38]. Current–voltage curves for this FET are shown in Figure 1.5. The top-gated geometry allows for a reduction in the voltage necessary to switch the device while allowing the integration of multiple devices on the same substrate. The high-*k* dielectric used in this device, HfO_2, also gave the additional benefit of improving the mobility of monolayer MoS_2 owing to dielectric engineering as discussed earlier[87,88,91,92]. Top-gating with a high-*k* dielectric was also used in a p-type FET with an active channel made of a monolayer flake of WSe_2, which exhibited room-temperature performance of ~250 cm^2 V^{-1} s^{-1} hole mobility, ~60 mV per decade subthreshold swing and 10^6 on/off ratio[93]. Thin-film transistors made of MoS_2

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from liquid exfoliation also have similar electrical performance[94], suggesting possibilities for flexible, transparent, 2D electronic applications. The development of CVD synthesis methods for obtaining large areas of MoS_2, as described earlier, is also important for wafer-scale fabrication of devices.

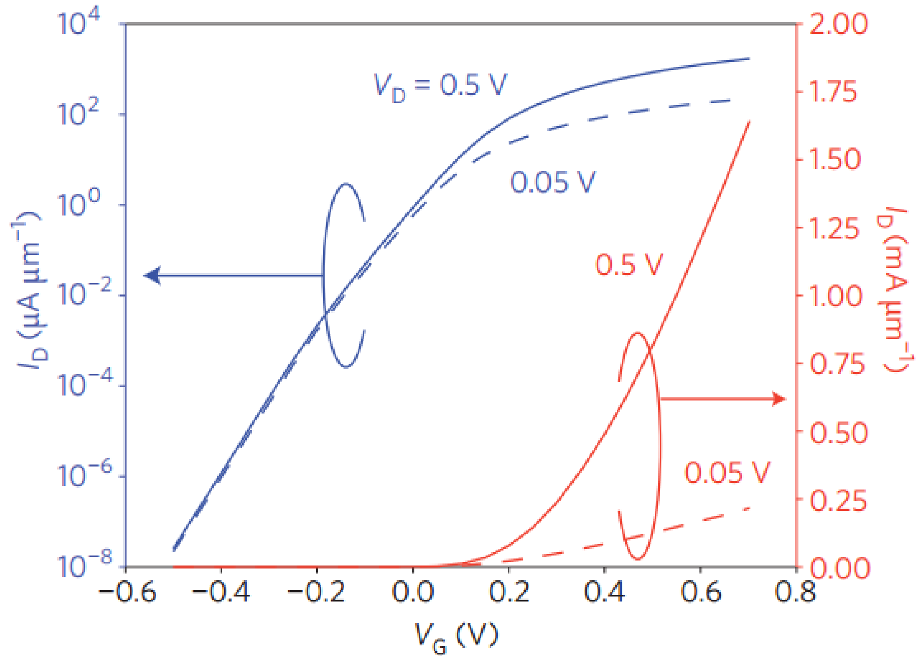

Figure 1.8: Simulated device characteristics for a monolayer MoS_2 FET device with 2.8-nm-thick HfO_2 top-gate oxide, 15-nm gate length, and power supply voltage 0.5 V[98]. The source–drain current (I_D) is plotted against gate voltage (V_G) for 0.05 and 0.5 V drain voltage (V_D) on linear (right axis) and logarithmic (left axis) scales.

Theoretical simulations of single-layer MoS_2 transistor performance[60,84] have quantified the expected resilience of MoS_2 to short-channel effects due to its atomic-scale thickness. These calculations show that top-gated MoS_2 transistors with gate lengths of 15 nm could operate in the ballistic regime with on-current as high as 1.6 mA μm^{-1}, subthreshold swing close to 60 mV per dec and current on/off ratio of 10^{10}. Simulated current–voltage curves for a single-layer MoS_2 transistor at different operating conditions are shown in Figure 1.8[84]. Although MoS_2 will not compete with conventional III–V

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transistors on mobility values alone, its attractive electrical performance characteristics, relatively high Earth abundance and high degree of electrostatic control could make MoS_2 a viable candidate for low-power electronics[84].

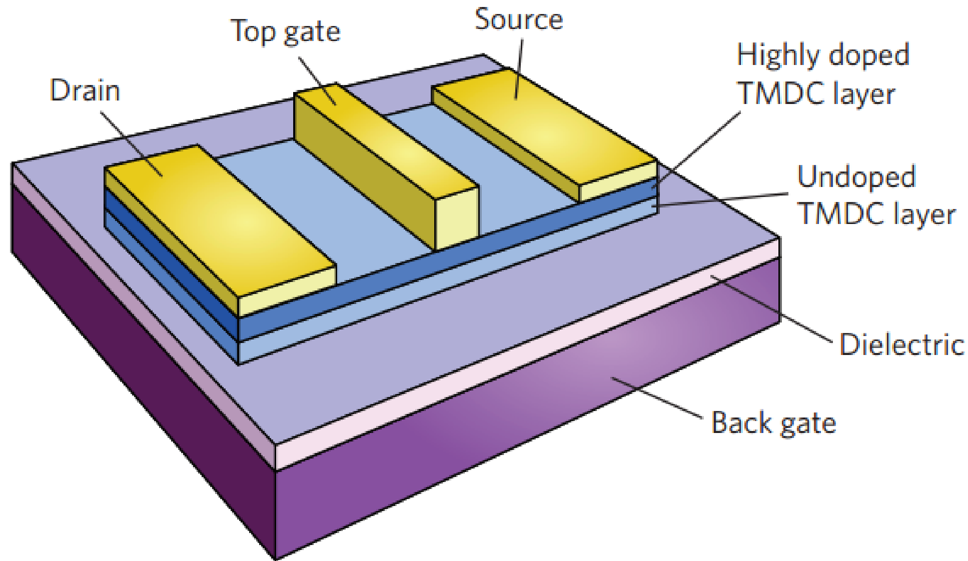

Figure 1.9: Proposed TMDC-based high-electron-mobility transistor (HEMT) device with top-gated Schottky contact and TMDC layers with different doping levels[20].

Radisavljevic *et al.*[31] recently demonstrated that they could build functional electronic circuits based on multiple 2D TMDC transistors capable of performing digital logic operations. Up to six independently switchable transistors were fabricated on the same piece of monolayer MoS_2 by lithographically patterning multiple sets of electrodes (Figure 1.6)[39]. An integrated circuit composed of two transistors fabricated on a single flake of MoS_2 was operated as a logical inverter, which converts a logical 0 into a logical 1, and as a logical NOR gate [39], which is one of the universal gates that can be built in combinations to form all other logic operations[95]. Wang *et al.* also recently demonstrated complex integrated circuits built on bilayer MoS_2, including an inverter, logical NAND gate, static random access memory and five-stage ring oscillator[96].

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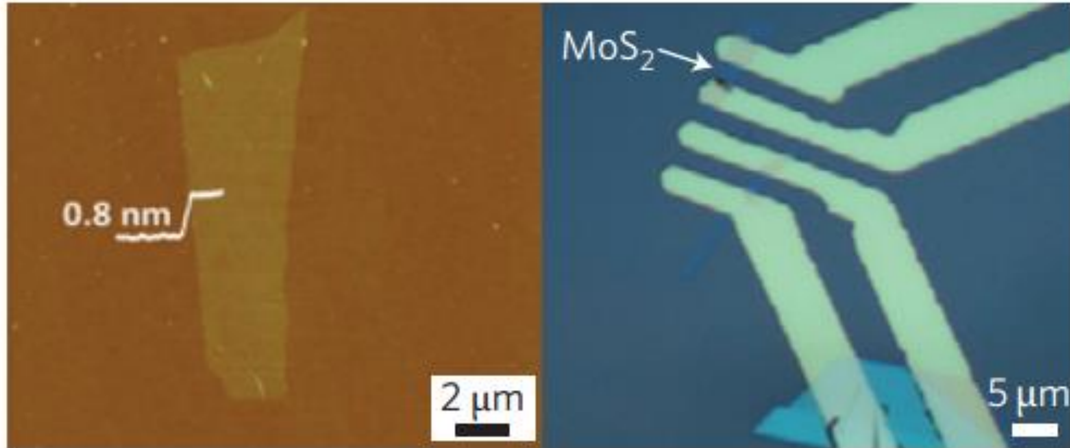

Figure 1.10: Atomic force microscopy image of MoS_2 monolayer flake (left) and optical microscopy image of this flake made into a device with metal contacts (right). The white trace in the left panel shows a height profile from AFM along the MoS_2 flake edge[114].

Ambipolar transport was demonstrated in a thin (10-nm-thick) MoS_2 electric double-layer transistor (EDTL) using an ionic liquid as the gate (Figure 1.6) to reach extremely high carrier concentrations of 1×10^{14} cm^2 [86]. The demonstration of both n- and p-type transport will be useful for applications like CMOS logic and p–n-junction optoelectronics. The on/off ratio was >200 in the device, but is much lower than the single-layer device described above[38], mainly because of the off-current passing through the bulk of the flakes[86]. The transfer curves (source–drain current as a function of gate voltage) for thin-flake and bulk MoS_2 ambipolar devices are shown in Figure 1.9.

1.4 2D Materials in Optoelectronics

The relatively high Earth abundance of TMDCs and their direct bandgaps in the visible range make them attractive as the light-absorbing material in alternative thin-film solar cells[97], including flexible photovoltaics that could coat buildings and curved structures. The workfunctions and conduction- and valence-band edges of several TMDCs are compatible with the workfunctions of commonly used electrode materials[98-

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100]. Moreover, the ability to tune the bandgap of TMDCs with various intercalants such as metal ions and organic molecules[101,102] may allow optical absorbances to be tuned in photovoltaic applications.

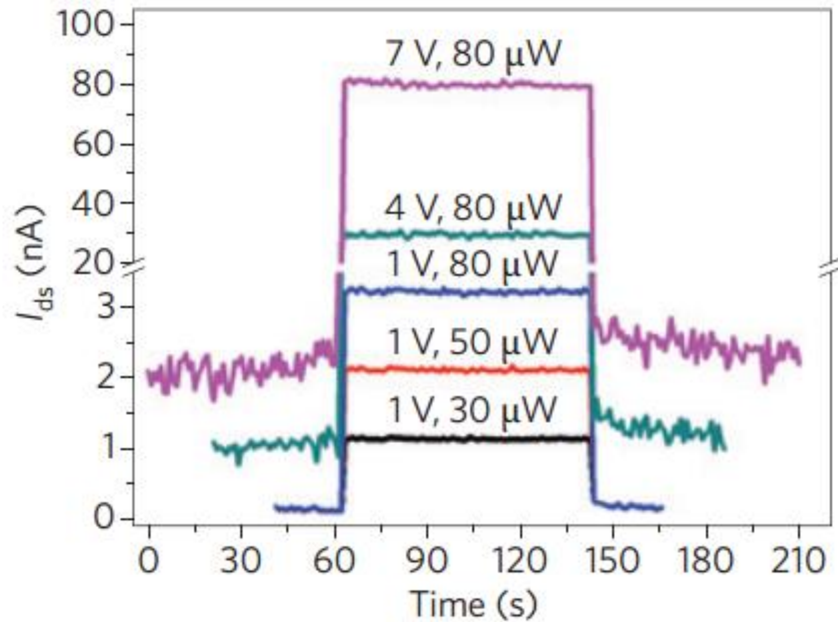

Figure 1.11: Photoswitching characteristics of single-layer MoS_2 phototransistor at different optical power (P_{light}) and drain voltage (V_{ds})[114].

A variety of roles for TMDCs in photovoltaics and photodetectors has been demonstrated. Thin films of MoS_2 and WS_2 are photosensitive[103], and a phototransistor made from a single layer of MoS_2 has shown its potential as a photodetector (Figure 1.10 and Figure 1.12)[114]. The photocurrent in this device depends on the incident light intensity, responds within 50 ms to changes in light levels and has high photoresponsivity. By using MoS_2 layers of different thicknesses, photodetection of different wavelengths can be tuned. Lee *et al*.[104] have demonstrated that single- and double-layer MoS_2, with respective bandgap energies of 1.8 and 1.65 eV, are effective for detecting green light, and triple-layer MoS_2 with a bandgap of 1.35 eV is well suited for red light. A bulk heterojunction solar cell made from TiO_2 nanoparticles, MoS_2 atomic layer nanosheets

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and poly(3-hexylthiophene) (P3HT) was recently demonstrated with 1.3% photoconversion efficiency[105]. Similarly, electrochemical solar cells with TiO_2 were sensitized with WS_2, which acts as a stable, inorganic absorber material[106,107]. TMDCs have also been demonstrated as conductors and electron-blocking layers in polymer LEDs[108,113].

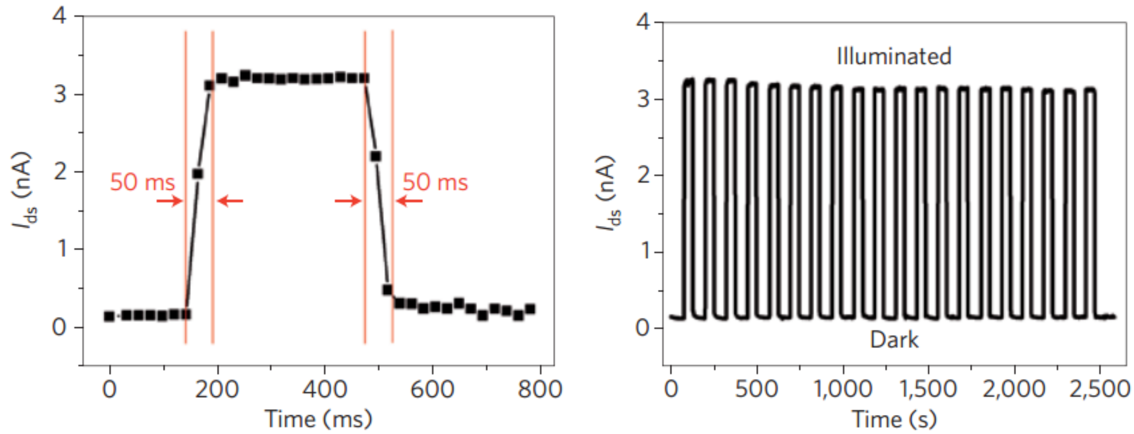

Figure 1.12: Photoswitching rate (left) and stability test (right) of photoswitching behaviour of single-layer MoS_2 phototransistor at V_{ds} = 1 V, P_{light} = 80 μW[114].

In Figure 1.13 and Figure 1.14, two proposed devices that incorporate materials with different bandgaps are shown: multijunction solar cells like these would allow photons of different energies in the full solar spectrum to be efficiently absorbed, reducing losses due to thermalization [109]. These structures could potentially be constructed using different TMDCs with varying bandgaps, which range from the visible to the near-infrared, as summarized in Table 1.1. The layer-dependent photodetector[104] discussed earlier demonstrates how light of different wavelengths can be preferentially absorbed by tuning the bandgap.

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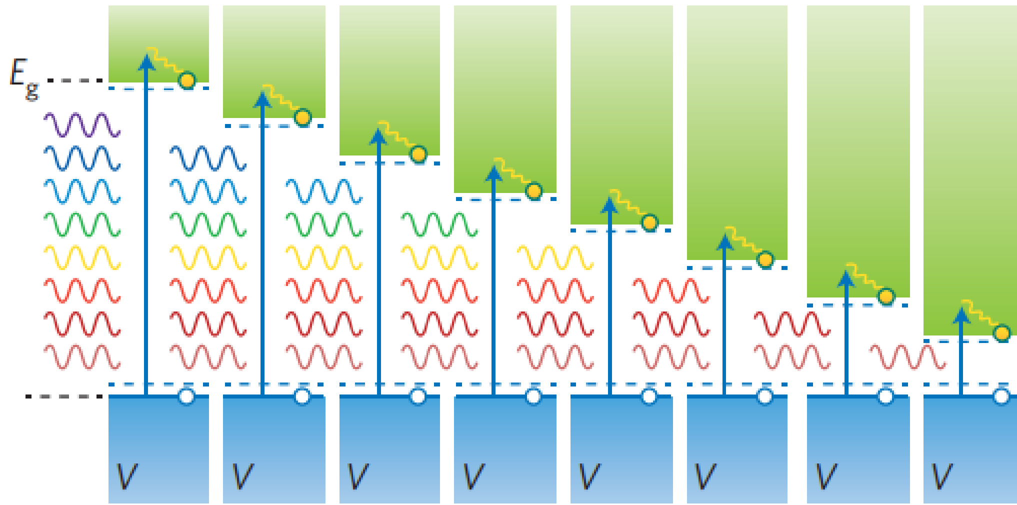

Figure 1.13: Energy-level diagram of proposed multijunction solar cell made of stacked semiconductors of different bandgaps to absorb different wavelengths from the solar spectrum to reduce thermalization losses. The blue dashed lines represent the quasi-Fermi levels defining the open-circuit voltage, and yellow dots represent electrons in the device[109].

Electroluminescence and photoluminescence are two important categories. In electroluminescence, photons are emitted in response to electrical stimulus; this mode is useful in optoelectronic devices such as LEDs and diode lasers. In photoluminescence, the material absorbs a photon and then re-radiates a photon, sometimes at a different energy. In direct-bandgap semiconductors, the radiative recombination of electrons and holes produces photons, and occurs much more efficiently than in indirect-bandgap semiconductors. The direct bandgaps of monolayer semiconducting TMDCs make them ideal candidates for the active light-emitting layer in future flexible optoelectronics, unlike graphene, which lacks a bandgap and requires chemical treatments to induce local bandgaps that photoluminesce [110,111]. Examples of electroluminescence in TMDCs include MoS_2 emitting light by electrical excitation through Au nano-contacts [112], and electroluminescence from SnS_2 exfoliated from lithium intercalation and incorporated into a composite polymer matrix[115].

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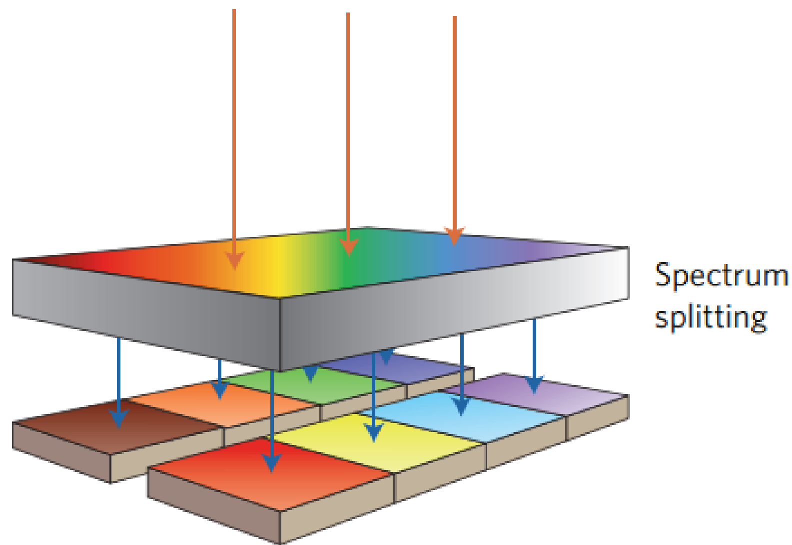

Figure 1.14: Proposed solar-cell device with parallel structures that may be fabricated using lift-off and printing techniques for patterning the semiconductor layers and a micro- or nanophotonic spectrum-splitting layer. The various bandgaps available from the different TMDCs are promising for use in such multijunction photovoltaic devices[20].

Photoluminescence is seen in monolayer MoS_2, which has a direct bandgap, and the quantum yield of the monolayer photoluminescence is much higher than for bilayer and bulk MoS_2[73,46]. As mentioned earlier, however, the photoluminescent quantum yield measured so far in MoS_2 is much lower than would be expected for a direct-gap semiconductor, and much work will be required to understand the photoluminescence emission and quenching processes before many feasible optoelectronic devices can be made.

1.5 2D Materials Used for Sensing

The electronic, optoelectronic and chemical properties of TMDs suggest opportunities in molecular sensing applications. As 2D materials, their high surface-to-volume ratio makes them particularly sensitive to changes in their surroundings. On exposure to gases and vapors, there can be changes such as charge transfer and doping,

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intercalation, and shifts in permittivity and lattice vibrations. For example, gas sensors from a graphene-based FET can perform with high sensitivity and low noise. The detection mechanism is due to adsorbed molecules transferring charge to the graphene sheet and changing its resistivity.[21]-[23] Changes to the electronic properties of TMDs caused by the presence of adsorbates can be detected electrically by incorporating the TMDs into transistor devices and measuring the current–voltage behavior, or optically by changes in the photoluminescence, absorbance or Raman spectra. For example, intercalation with Li^+ ions causes an upshift in the MoS_2 Raman A_{1g} and E^1_{2g} peak positions and a decrease in peak intensities, probably owing to strain introduced by the Li^+ entering interstitial sites.[24],[25] The photoluminescence of monolayer MoS_2 also suggests applications in biosensing, where stable fluorescent markers are of importance for imaging and fluorometric assays.

Transistors made from single- and few-layer MoS_2 sheets have been demonstrated to be sensitive detectors for NO gas.[26] The detection mechanism is probably due to p-doping induced by the adsorbed NO, changing the resistivity of the intrinsically n-doped MoS_2. Similarly, flexible thin-film transistors with active regions composed of MoS_2 generated from the electrochemical lithiation and exfoliation technique[27] have been demonstrated as sensitive NO_2 gas detectors.[28] Thin-film humidity sensors made from liquid-phase exfoliated VS_2 nanosheets have been incorporated into a sensor array that can detect the moisture from fingers.[29] The conductivity in these sensors is modulated by the presence of water molecules, which inhibit conduction along V atoms at flake edges.[29] Transistors made from MoS_2 also exhibit humidity-dependent hysteresis in their current–voltage behavior, probably owing to water molecules easily adsorbing onto the

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hydrophilic MoS_2 surface and being polarized by the applied gate voltage.[30] Finally, MoS_2 flakes incorporated into a glassy carbon electrode in an electrochemical cell can be electrochemically reduced, and this reduced material has been shown to have electrochemical sensitivity toward glucose and biomolecules such as dopamine.[31]

1.6 Dissertation Outline

In Chapter 1, an overview of the applications of TMDs are given to highlight the importance of this growing branch materials. The motivation of this work lies in the fact that heterojunctions of various materials allow us to take advantage of there individual properties, and that is only possible when the constituents are very thin. This discussion is resumed in Chapter 3, where heterojunctions with graphene are discussed to demonstrate how far the field has advanced so far.

In Chapter 2, we start the discussion with a novel transferr-free synthesis technique of MoS_2 thin films. Later on, transistor characterization results are shown to highlight the performance of this material as a suitable candidate for making high performance field effect transistors.

Chapter 4 presents a graphene/MoS2 barristor with excellent barrier height tunability, and its application as high gain phototransistor. The discussion continues to Chapter 5, where we show chemical/gas sensing results to demonstrate the versatile applications of this device. In Chapter 6, a graphene/InN nanowire based mixed dimensional barristor is presented with a wide range of applications – trace gas detection with sub-ppb detection limit, photo-detection with very high responsivity and gate controllable memristive action. Finally, in Chapter 7, a summary of the dissertation is presented along with suggested future research works.

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Chapter 2

Synthesis and Characterization of MoS_2 thin Films

In this chapter, we demonstrate a transfer-free method for producing 3-5 monolayers (ML), large area MoS_2 by pre-oxidation of metallic Mo. The growth temperature was reduced, eliminating free sulfur-induced degradation of the SiO_2 gate dielectric. The pre-oxidation step produces chemically active mixed oxides, which can then be readily sulfidized without requiring a high temperature slfidation for longer duration. As a result, the oxide leakage is substantially reduced, while producing a fine quality MoS2 thin film with excellent transistor characteristics.[29] The effect of temperature on career transport has also been discussed in terms of current-voltage and capacitance-voltage measurements.

2.1 Synthesis of MoS_2 via pre-oxidation

We developed a top-down growth technique for synthesizing large area, few atomic layer thick MoS_2 transistors. The process oxidizes patterned metallic Mo to form a mixture of volatile Mo-oxides and thin the resulting film down by partial sublimation at a low temperature. Eventually sulfur vapor is introduced to the system to sulfidize the volatile oxides to MoS_2 at relatively low temperature (<500 ^oC). One advantage of the low growth temperature is to avoid contamination of SiO_2 by diffused sulfur atoms, which allows the as-grown films to be used without transferring to different substrates, while maintaining the state-of-the art transistor characteristics on SiO_2.

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2.1.1 Growth and Fabrication

The high quality MoS_2 samples were grown on 50 nm SiO_2/n^+-Si commercial substrate. A lithographic process was first performed to open up sub-mm sized rectangular windows on a clean SiO_2/Si sample, followed by the electron beam evaporation and lift-off of a 7-10 nm thick layer of Mo. This thick layer, if fully sulfidized, would have led to a >20 ML (monolayers) thick MoS_2. However, the 7-10 nm was the minimum thickness required to form a continuous film rather than islands on SiO_2, necessitating the post-growth thinning described below. The sample was placed on a quartz boat inside the high temperature region of a two-zone horizontal tube furnace. 10 mg of sulfur powder (Fisher Scientific, 99.99% purity) was placed on a quartz plate in the colder region of the process tube (Figure 2.1).

Figure 2.1: Tube furnace, temperature and mass flow controller systems used for MoS_2 synthesis.

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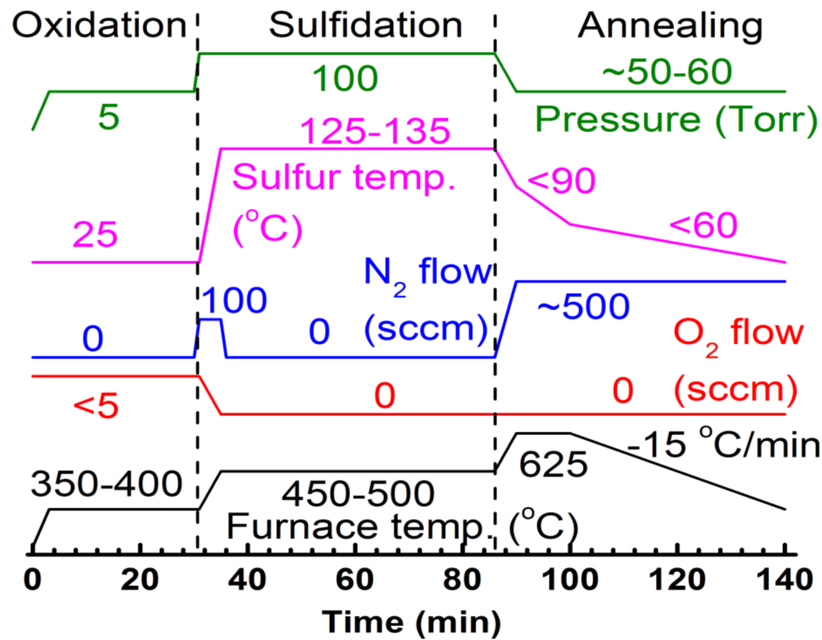

Figure 2.2: Temperature, pressure and gas flow rates during various stages of the growth of MoS_2. The Y-axis is not to scale and the plots are shifted vertically for clear understanding.

The tube was pumped down to rough vacuum and purged with ultra-high purity (UHP) N_2 before the growth started. The synthesis process was completed in three steps; a pictorial representation of the process flow is provided in Figure 2.2. The first step was to oxidize the Mo sample at 350-400 ^{o}C for 25-30 minutes in a low O_2 flow (~5 sccm) before sulfidation to form volatile Mo-oxides, and thin down the Mo-containing film by partial sublimation. In step two, the hot zone temperature was raised to 450-500 ^{o}C and the cold zone temperature was elevated to 125-135 ^{o}C to allow the melting of sulfur while the O_2 flow was gradually tapered off. No carrier gas was flowed during this step for ~50 minutes, during which the sulfur vapor reacted with the MoO_x and formed MoS_2. In the final step, the cold zone temperature was reduced below the melting point of sulfur to quench the sulfidation, while the hot zone temperature was quickly raised to 625°C for 10 more minutes, with a high flow of dry N_2 to improve the crystal quality, complete the sulfidation reaction and remove the residual sulfur vapor from the reactor. Finally, the

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entire furnace was slowly cooled down to room temperature (-15 ^{o}C/min) in presence of the same N_2 flow. The sample was then taken out from the chamber and was annealed in a separate process tube at 1000 ^{o}C in N_2 ambient for 30 minutes to improve crystallinity and electronic property, in agreement with others.[1],[6] Metal contacts, Ti/Au of 20/80 nm thicknesses formed by lift-off, were sintered at 350-400 ^{o}C for 60 minutes in N_2 ambient.

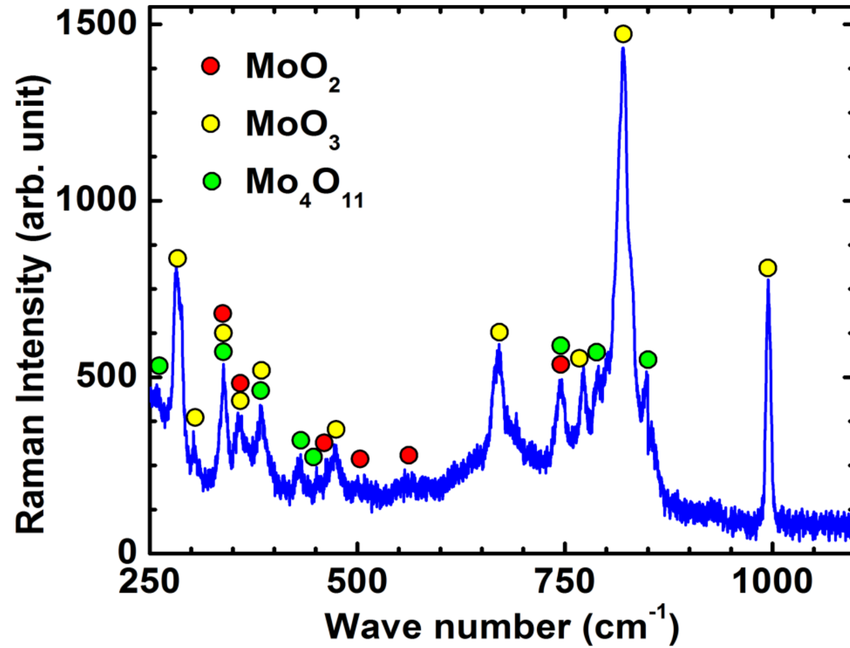

Figure 2.3: Raman spectra of oxidized pre-growth Mo samples showing peaks for various oxides of Mo.[7]

2.1.2 Post-growth Characterization

The initial low temperature baking of the sample in presence of O_2 (first step of the growth process) forms various volatile oxides of Mo, as confirmed by the Raman spectra of a sample that was taken out of the chamber after the initial oxidation phase. The spectra, as shown in Figure 2.3, indicates characteristic peaks of MoO_2, MoO_3 and an intermediate Mo-oxide, Mo_4O_{11}.[7] This was inspired by previous reports on the synthesis of MoS_2, directly from either MoO_2 or MoO_3, since these oxides were shown to sulfidize more readily than pure Mo metal.[8],[9] Here, we expand on this concept by oxidizing Mo

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by a very limited O_2 flow at a low temperature, which forms poor quality, O-deficient oxides with many chemically active sites at dangling bonds, leading to the mixed oxides observed.

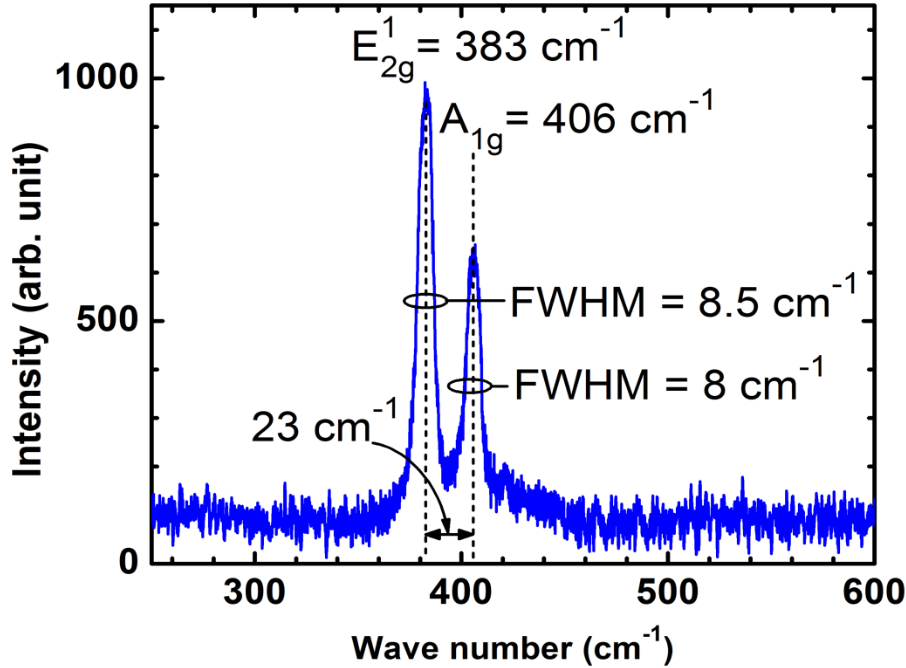

Figure 2.4: Raman spectra of MoS_2 with E^1_{2g} peak at 383 cm^{-1} and A_{1g} peak at 406 cm^{-1}; the separation of the peaks is 23 cm^{-1}, which is generally observed in 3-5 ML MoS_2.[5] All the peaks from MoO_x are undetectable after sulfidation, indicating a total conversion of all such oxides.

The Raman spectra of the optimized as-grown MoS_2 sample is shown in Figure 2.4, where the characteristic A_{1g} and E^1_{2g} peaks are observed to be separated by 23 cm^{-1}, indicating 3-5 ML thick MoS_2 (2-3 nm).[5] The Mo-oxide peaks shown in Figure 2.3 disappeared entirely after the sulfidation process, which indicates complete conversion of Mo-oxides to MoS_2. The reduction of thickness during the growth process (from 7-10 nm Mo to 3-5 ML MoS_2) is attributed to the sublimation of the volatile MoO_x during the onset of sulfidation. A tapping mode atomic force microscopy (AFM) image taken on a Veeco DI3000 AFM is also shown in Figure 2.5 which shows a film thickness of 1.7 nm and root mean square surface roughness of <0.4 nm.

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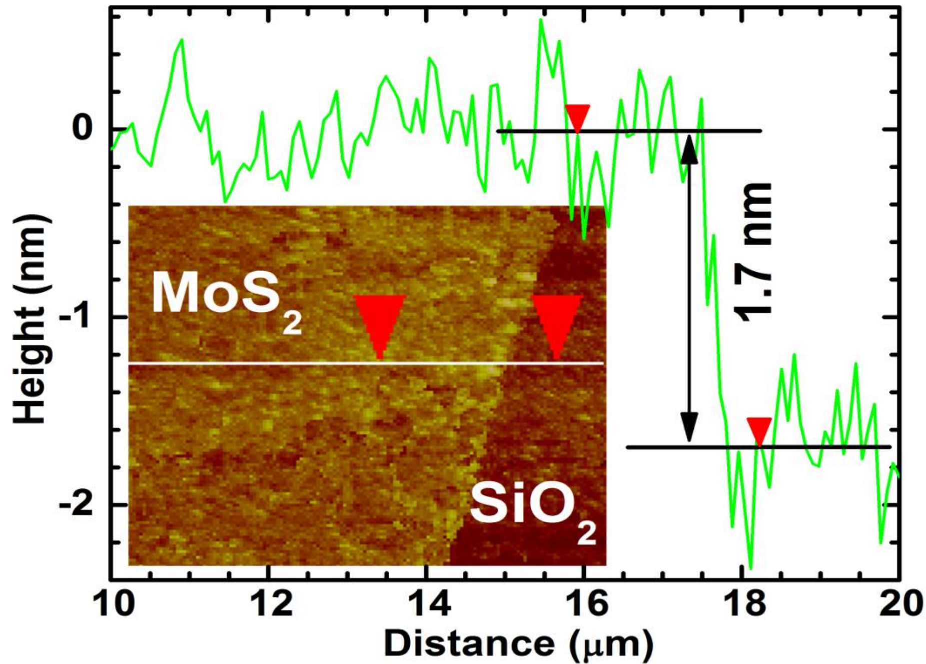

Figure 2.5: Tapping mode atomic force microscopy image of MoS_2 on SiO_2 (inset) with a step height of 1.7 nm along the edge of the MoS_2 film, corresponding to ~3ML, in agreement with the Raman results.

To further demonstrate the usefulness of the proposed multi-step growth process, we compare it with a direct sulfidation method where the first two steps of the growth (oxidation at < 400 ^oC and sulfidation at <500 ^oC) were skipped and a higher temperature (700-800 ^oC) was used for the single step sulfidation process instead. Due to the absence of growth-time thinning process, a much thicker MoS_2 film was formed with several serious drawbacks: (1) thicker MoS_2 had to be thinned and (2) the SiO_2 was irreversibly damaged due to the exposure to elemental sulfur vapor at high temperature (Figure 2.6). While laser ablation,[10] plasma treatment[11] and thermal annealing[12] have been shown to effectively thin the MoS_2, it would still be unusable until the MoS_2 film was transferred to a fresh SiO_2/Si substrate due to this degradation. Thus, by reducing the sulfidation temperature through a pre-oxidation step instead of using the direct sulfidation method (longer duration at higher temperature), the gate leakage current was reduced by

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as much as 10^8, while simultaneously limiting the thickness to <5ML, with a bandgap of 1.4 eV.[13] The gate leakage current is much less than the drain current for all gate voltages (Figure 2.16), showing that the gate breakdown has been effectively suppressed. Since both samples shown in Figure 2.16 had identical substrates at the beginning of the growth, this comparison clearly shows that the proposed method preserves the dielectric quality while the other method does not.

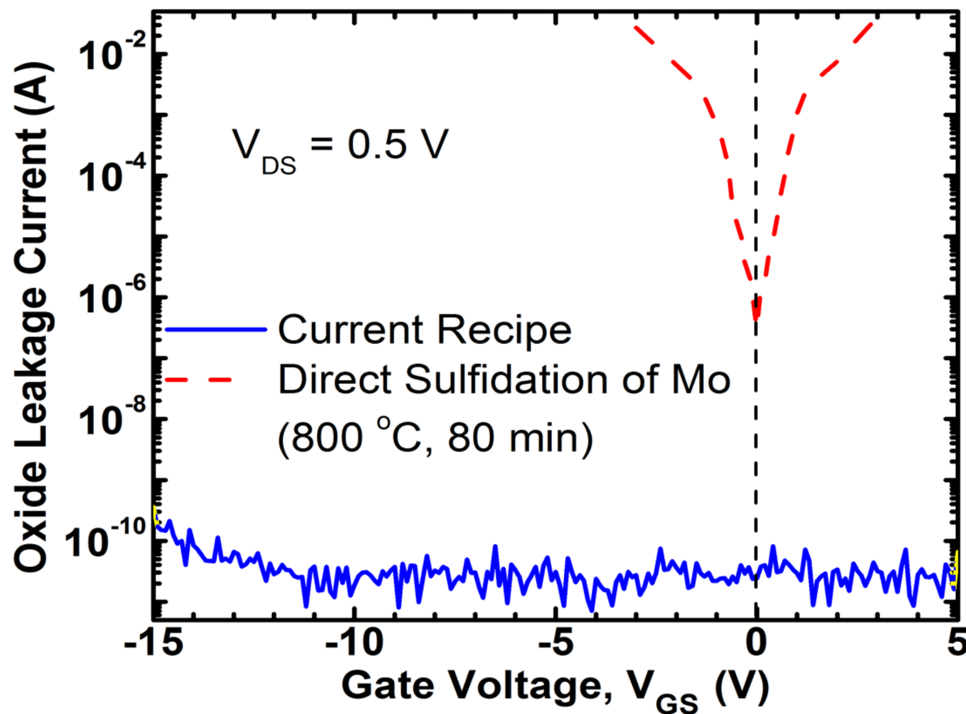

Figure 2.6: Magnitude of gate leakage current through the SiO_2 layer at V_{DS} = 0.5 V, using current three-step recipe and an alternative recipe with one-step direct sulfidation at high temperature. The insulating property of SiO_2 is severely compromised during direct sulfidation of Mo.

2.2 Characterization of MoS_2 FET

The MoS_2 based back-gated FET's were characterized on a probe station with a temperature controlled chuck (300-500K) to study the effect of temperature on the current-voltage (I-V) characteristics using an Agilent B2902 source measuring unit (SMU) and capacitance-voltage (C-V) characteristics using a HP4284A precision LCR meter.

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The schematic of the device structure is given in Figure 2.7.

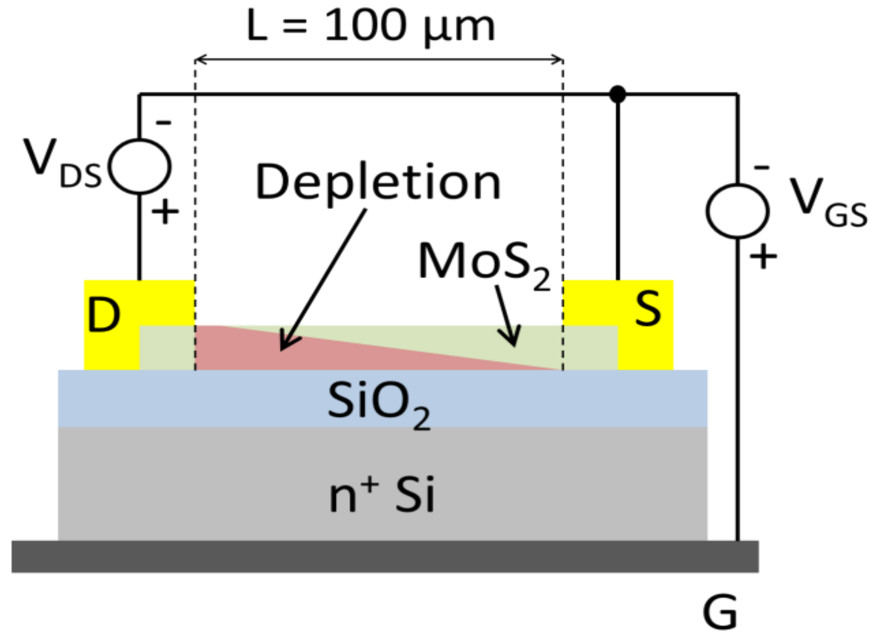

Figure 2.7: Schematic of the device, showing the electrical test configuration and the pinching-off of the channel by the depletion region at $V_{DS} > V_{DS,sat}$.

2.2.1 Capacitance-Voltage (C-V) Measurements

Figure 2.8 shows the measured FET capacitance, C_{FET} vs V_{GS} curves for temperatures 300-500K at 1 kHz, demonstrating the shape of a classical MOS capacitor. For $V_{GS} > 0$ V there is an accumulation of electrons, while $V_{GS} < 0$ V causes the channel to be depleted of free electrons, eventually causing strong inversion below -12V. C_{FET} in accumulation approaches a value of ~0.064 μF/cm^2, corresponding to an oxide thickness, t_{ox}, of about 54 nm, consistent with the nominal value of 50 nm. In inversion, the C_{FET} approaches a value ~60% smaller because of the series resistance seen by the holes in inversion, which agrees with the limited drain current in inversion (Figure 2.11 - Figure 2.16), as well as the band structure, and will be discussed further below. The residual C_{ox} for $-10.5V<V_{GS}<-7V$ is due to the limits of the measurement setup. The small increase with temperature is due to the contacts becoming more conductive, reducing the series

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resistance in the circuit, again consistent with the I-V characteristics below. The inset of Figure 2.8 shows the C-V curves at 300 K with back and forth sweeping of the V_{GS}, where the identical curves for both sweep directions indicate the absence of hysteresis.

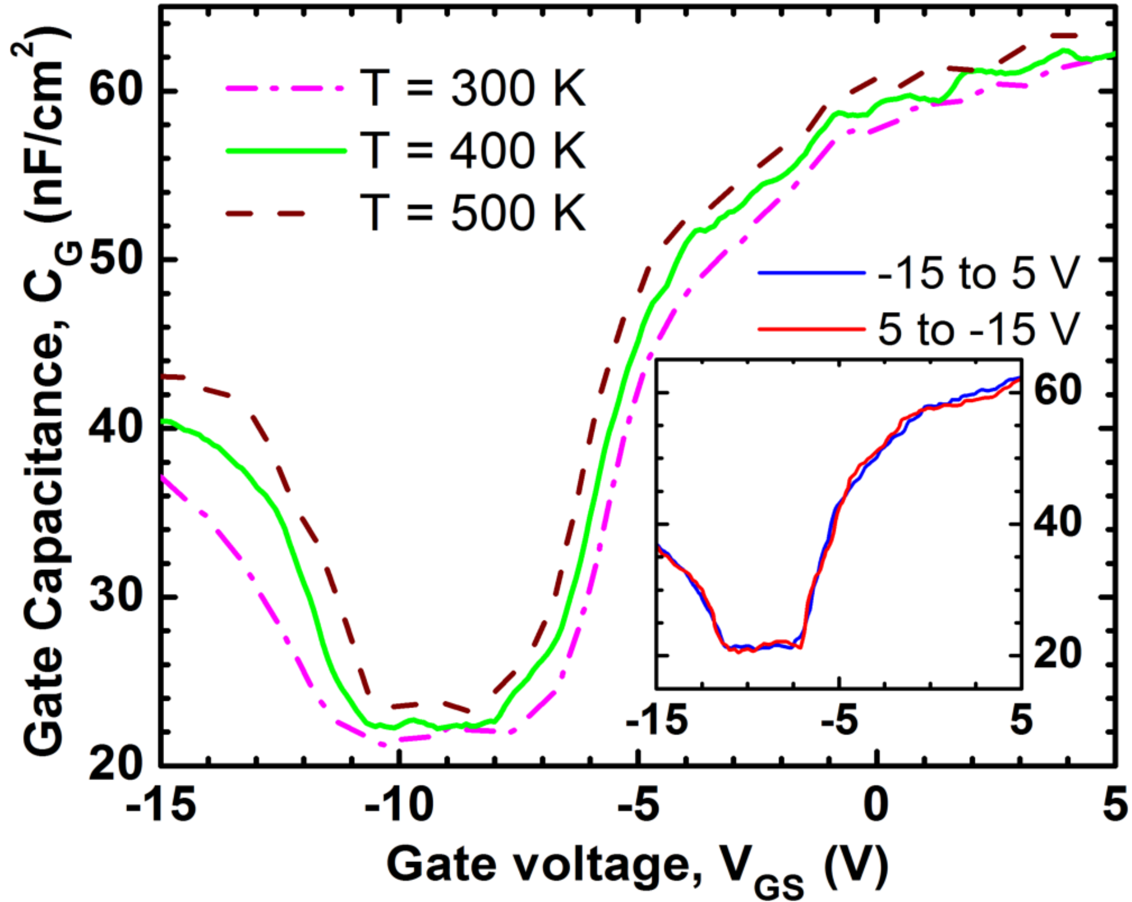

Figure 2.8: Gate capacitance-voltage (C-V) characteristics of a MoS_2 FET showing charge accumulation, depletion and inversion with different gate voltage biases and temperatures. The inset shows C-V curves using alternating sweep directions without any sign of hysteresis.

We determine V_{FB} using the following relation that relates $1/C_G^2$ with V_{GS}[14] –

$$\frac{1}{C_G^2} = \frac{1}{C_{ox}^2} + k(V_{GS} - V_{FB}) \quad (1)$$

where k is a constant depending on the unintentional doping concentration and dielectric constant of MoS_2.

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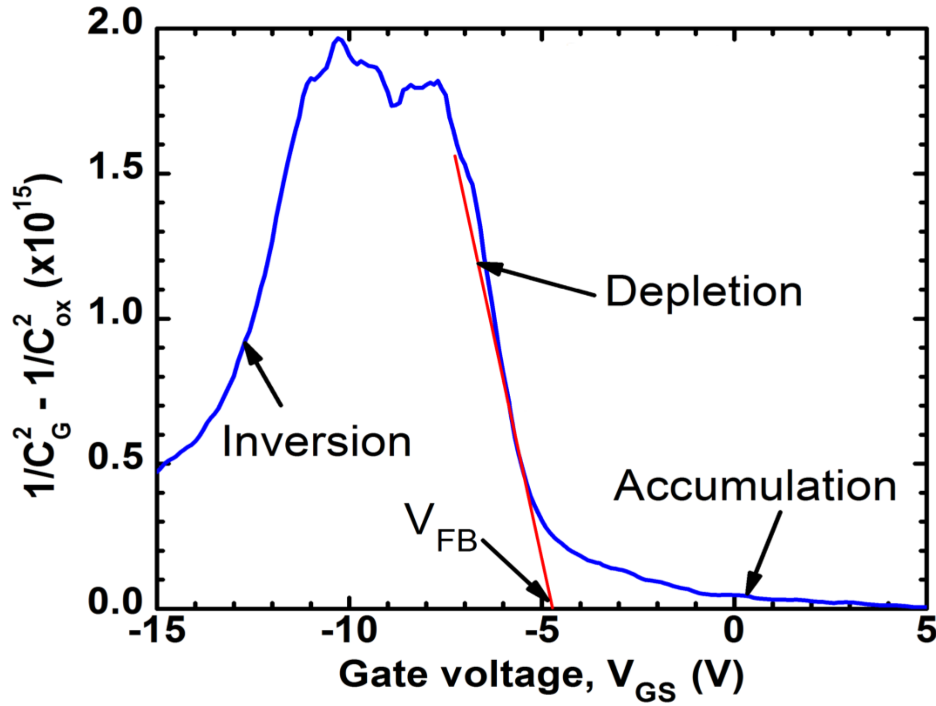

Figure 2.9: Estimation of flat band voltage (V_{FB}) using the $1/C^2$ vs V_{GS} curve near the knee point of the depletion region.

In Figure 2.9, we plot $1/C_G^2 - 1/C_{ox}^2$ as a function of V_{GS} and perform a linear fit at the depletion region. The V_{FB}, marked by the X-axis intercept of the fitting line, is estimated to be -4.8 ± 0.2 V. This V_{FB} shows a significant shift from the -1 V value estimated from the work function difference between MoS_2 and Si, and as reported by others.[1],[6] This shift in voltage can be attributed to positive interface charges, the density of which is calculated by, $n_{int} = \Delta V_{FB}\, C_{ox}/q \approx 2\times10^{12}$ cm^{-2}. The charges are considered to be fixed charges, and not traps, since no hysteresis was observed in the I-V nor in C-V. This n_{int} is very low for a non-native oxide-semiconductor interface, where even for native interfaces, n_{int} can approach 10^{13}cm^{-2} (e.g. [15]). The corresponding band diagrams are shown in Figure 2.10. These charges are attributed to this transfer-free growth process, and are crucial to describing the I-V characteristics below.

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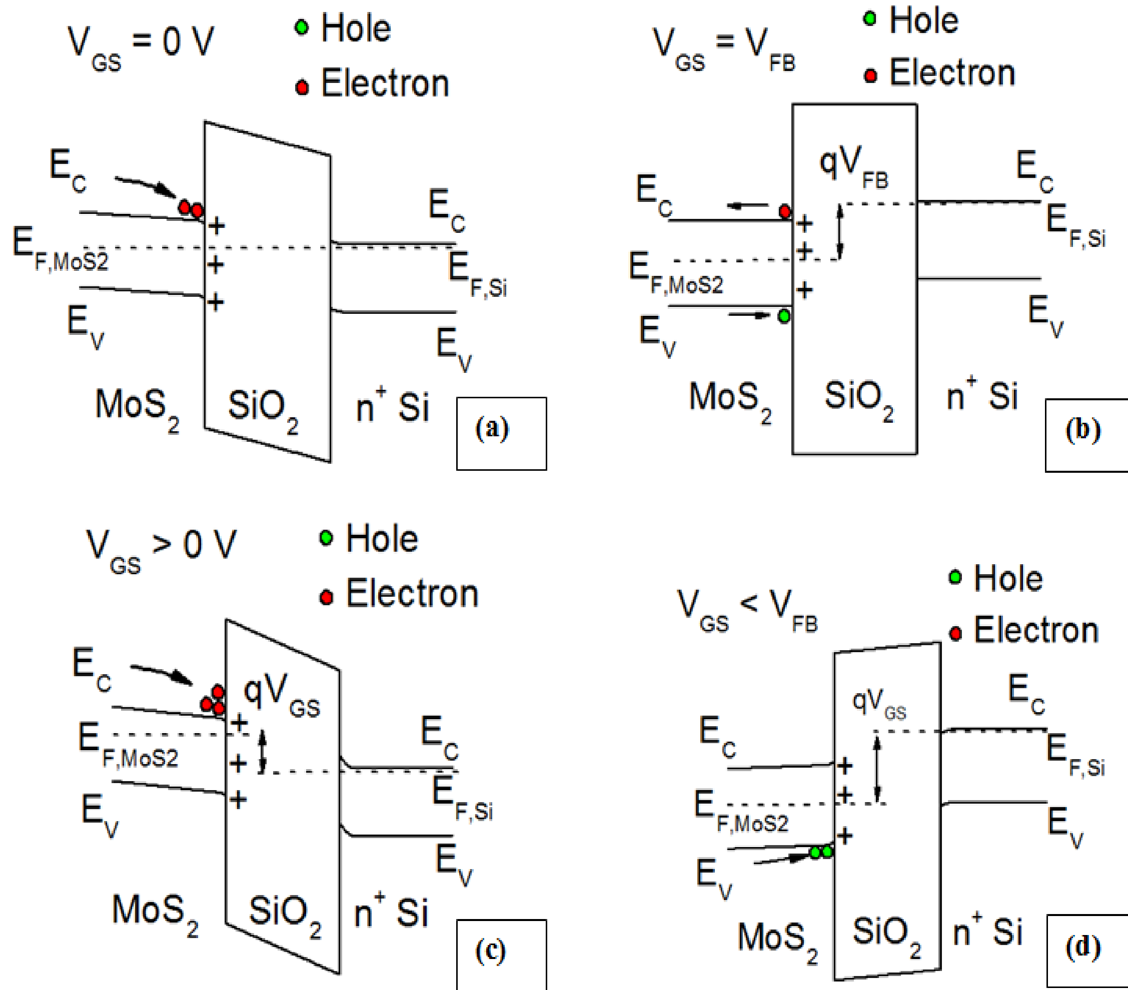

Figure 2.10: Energy band diagrams of the MoS_2-based MOS capacitor structure at different bias ranges. (a) At thermal equilibrium, electrons are pulled near the MoS_2/SiO_2 interface by the electric field established by the interface charges and the work function difference between Si and MoS_2. (b) At $V_{GS} > 0$ V, more electrons accumulate. (c) The opposite event takes place at depletion (e.g. $V_{GS} = V_{FB} < 0$ V) regime where electrons are repelled and holes are attracted, thus flattening the band. (d) At $V_{GS} < V_{FB}$ inversion regime takes place, where the energy bands bend to such extent that the material acts like a p-type semiconductor and accumulates holes.

2.2.2 **Current-Voltage (I-V) Measurements**

Figure 2.11 shows the transfer characteristic at $V_{DS} = 0.5$ V, a region in which the FET is in the triode region for all ranges of V_{GS} (Figure 2.16). The linear plots of I_D, as shown in the inset of Figure 2.12, were used to determine the threshold voltages (V_T). At $V_{GS} = 0$V, the transistor is normally on, showing electron conduction in accumulation,

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with a threshold voltage, V_T of about -8.8 V, and an ON/OFF ratio of about 10^5.

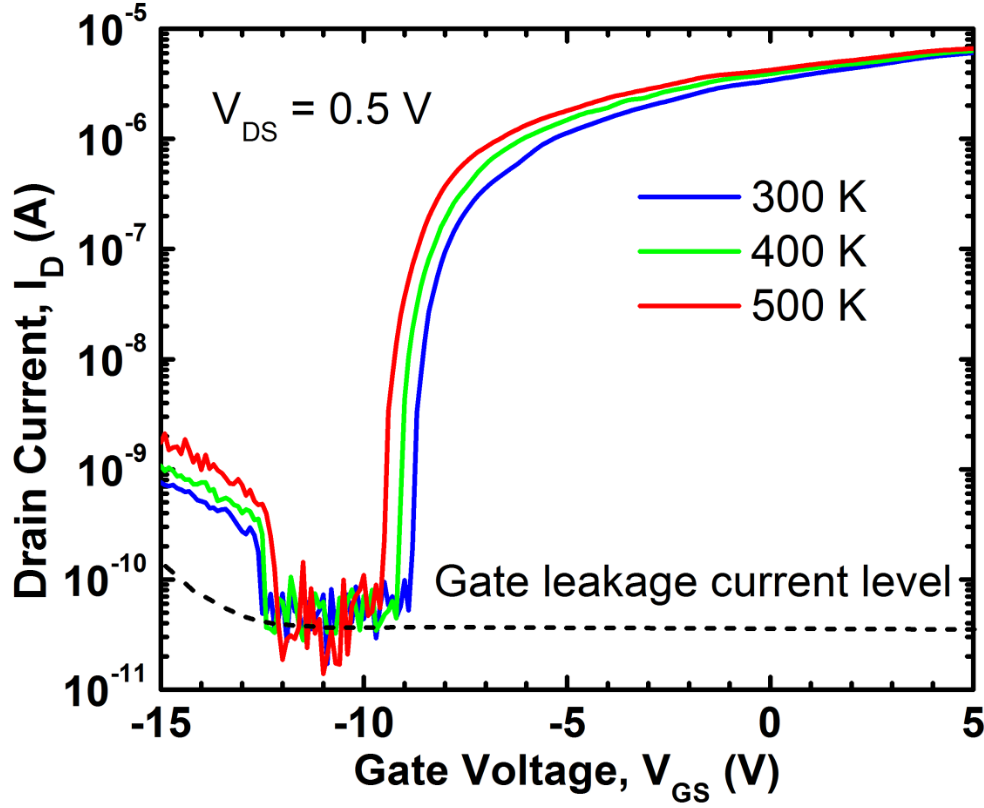

Figure 2.11: Transfer characteristics of MoS_2 based FET with W=20 μm, L = 100 μm and V_{DS} = 0.5 V, showing drain current as a function of gate voltage at different temperatures.

The accumulation subthreshold swing (SS) is 84 mV/decade which, along with the mobility mentioned below, is among the best for synthetic MoS_2 devices, indicating the robustness of the gate dielectric to the growth process. The field effect mobility μ_{FET}, is estimated from the linear FET characteristics:

$$\mu_{FET} = \frac{g_m L}{W V_{DS} C_{ox}} \quad (2)$$

where the transconductance $g_m = \partial I_D / \partial V_{GS}|_{VDS=0.5\ V}$, L is the channel length, W the width of the FET, while C_{ox} is the oxide capacitance per unit area. Here, we use the C_{ox} measured in Figure 2.8. In Figure 2.13, we show the transconductance (g_m) vs. V_{GS} curves at various V_{DS} between 0.5 and 2.5 V. These curves are used to calculate the

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mobility values of MoS_2 based FET and the peak value of μ_{FET} = 84 $cm^2/V.s$ is estimated at accumulation.

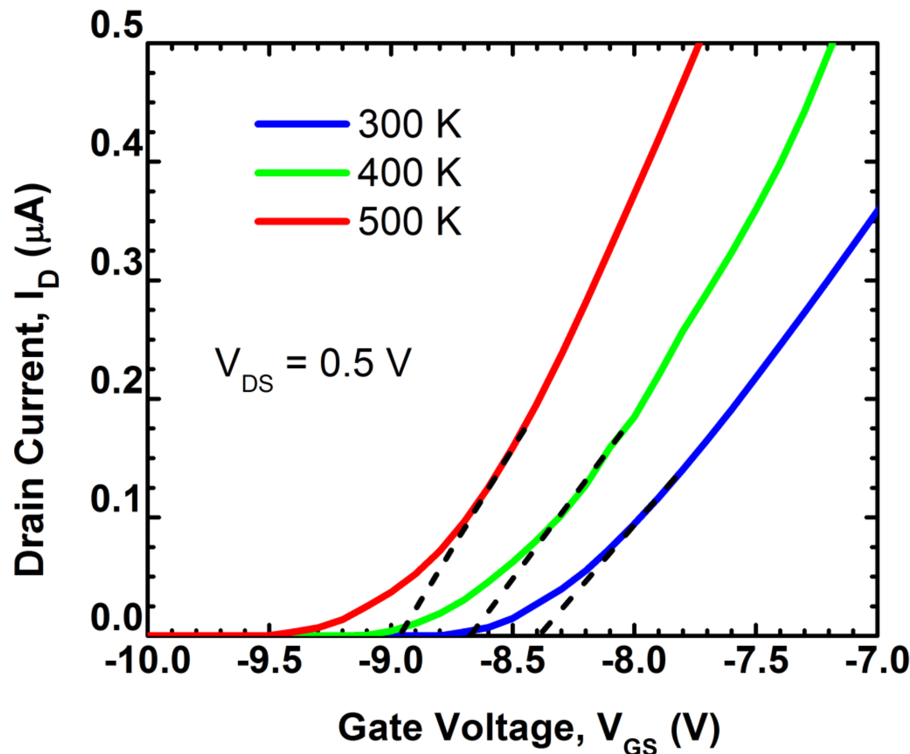

Figure 2.12: The linear I_D vs V_{GS} curves for the same data as shown in Figure 2.11, showing the threshold voltage, V_T's, determined by the X-axis intercept of the dashed tangent lines .

In Figure 2.14, we show a transfer curve at V_{DS} = 2.5 V to verify the absence of hysteresis in the I-V characteristics. Here the sweep was performed in both directions and the resulting curves overlap with each other. This dataset is arbitrarily chosen and is representative of all other bias conditions, which too did not show any sign of hysteresis.

The mobility decreases weakly as the temperature increases (Figure 2.11 and Figure 2.19), which is attributed to the canceling of the ionized impurity scattering (μ_{FET} increases with T), with phonon scattering (μ_{FET} decreases with T), as has been reported by others.[6] V_T also decreases with temperature at a rate of ~4 mV/K (Figure 2.12), consistent with the calculations for thick oxide MOSFET's.[16]

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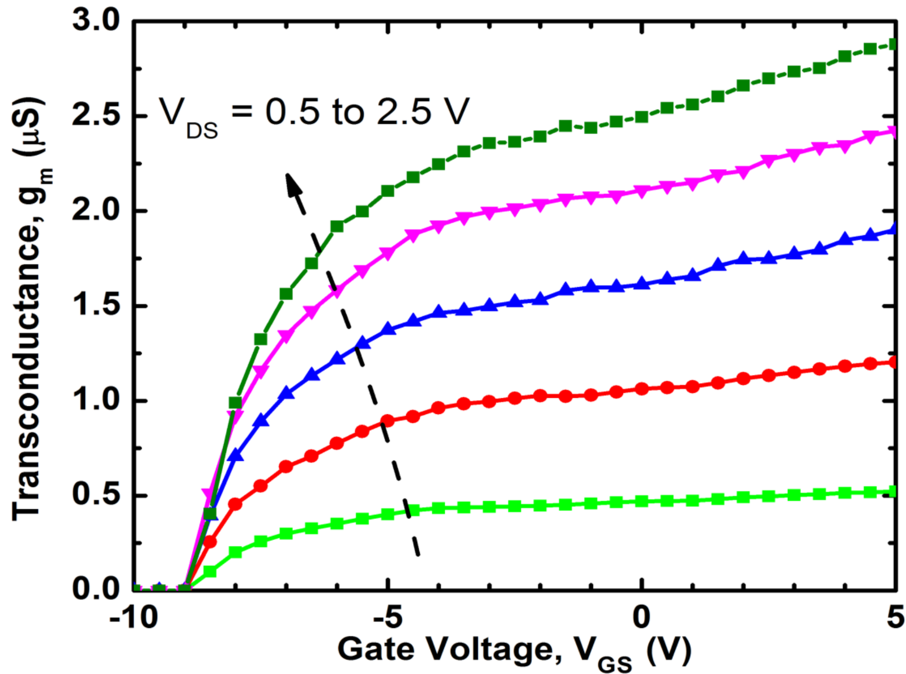

Figure 2.13: Transconductance curves at different drain bias voltages (V_{DS}) between 0.5 V and 2.5 V.

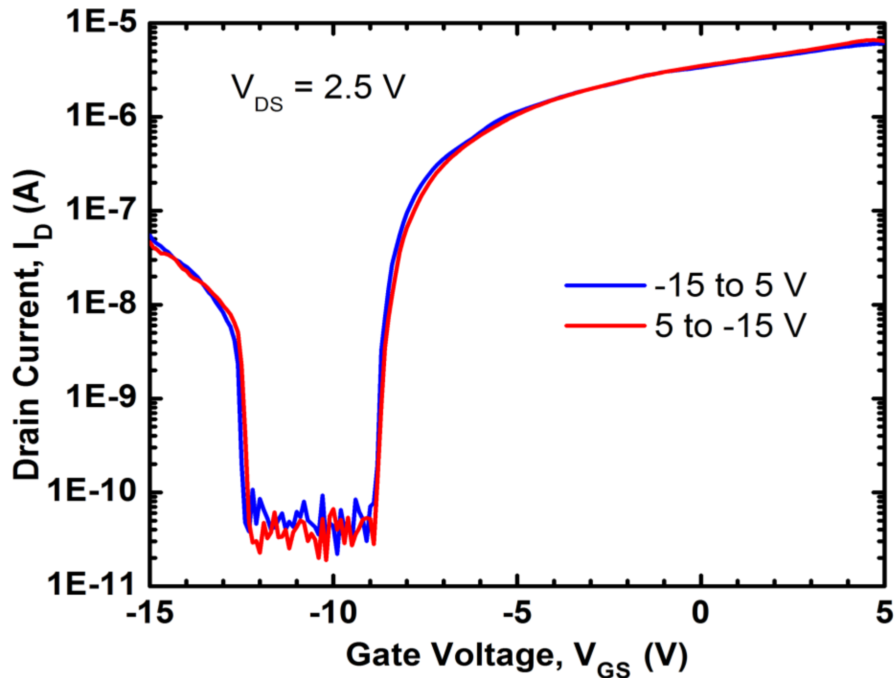

Figure 2.14: Transfer curves at V_{DS} = 2.5 V measured with the gate bias swept from -15V to 5 V and 5 V to -15 V. The identical transfer curves in both sweep directions indicate the absence of hysteresis.

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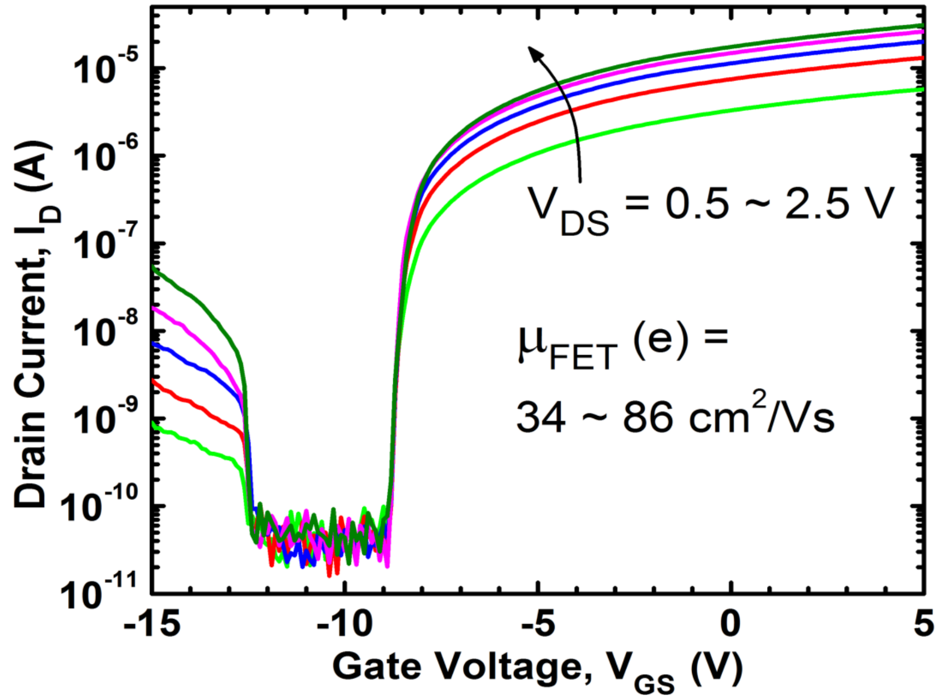

Figure 2.15: Transfer characteristics with drain voltages from 0.5 V to 2.5 V to show the effect of V_{DS} at T=300K.

Figure 2.15 shows the transfer curves measured at varying V_{DS} at 300 K. As V_{DS} increases from 0.5 V to 2.5 V, the electron mobility increases. Figure 2.16 shows the I_D vs V_{DS} family of curves for -8 V $< V_{GS} <$ 4 V in accumulation, and -13 V $< V_{GS} <$ -15 V in inversion, where the current is normalized by gate width (20 μm). The first set of curves (solid lines, up to V_{DS} = 5 V) are for $V_{GS} > V_T$, where V_T is the threshold voltage of the FET, located at around -8.5 V. These curves have two distinct regions: a typical linear triode regime followed by a saturation regime that varies with V_{GS}. For a channel with only a few atomic layers, this device carries a large amount of current (> 1 mA/mm), limited by the contact resistance of 1-4 kΩ which was measured by transmission line measurements (TLM) [17].

The contact resistance was measured using transmission line measurements (TLM), where contact pads were formed on a rectangular strip of MoS_2 on SiO_2/Si at

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linearly varying intervals. The resistance between each two consecutive pads were measured in presence of a fixed back-gate bias and plotted as a function of channel length (i.e. separation of pads) as shown in Figure 2.17. Using linear regression, the Y-axis intercept was obtained for each case, which equaled to $2R_c$, with R_c being the contact resistance. The pads were 100 μm in width, same as the FETs used in the work. Figure 2.18 shows the variation of R_c as a function of back gate bias in depletion-accumulation region.

The maximum electric field in the channel is calculated to be less than 500 V/cm at V_{DS} = 5 V, which is far smaller than the critical field for MoS_2 as found in the literature.[18] As a result, the drift velocity is calculated out to be ~10^4 cm/s, using the carrier concentration obtained from C-V, and the extracted μ_{FET} (discussed later).

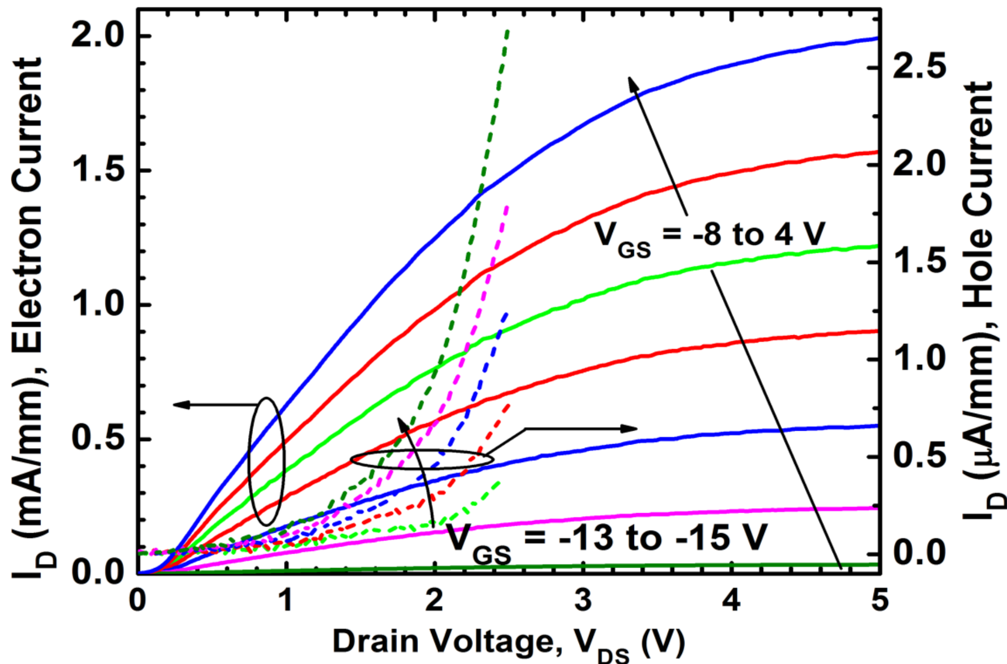

Figure 2.16: Normalized T=300K I_D-V_{DS} characteristics of the back-gated MOS_2 FET with respect to gate voltage V_{GS}, shown in two distinct regimes. The first one ranges from -8 to 4 V with electrons being the majority carriers. The second regime (dashed curves, V_{GS} = -13 ~ -15 V) shows highly non-linear trends in the inversion regime with holes being the majority carriers.

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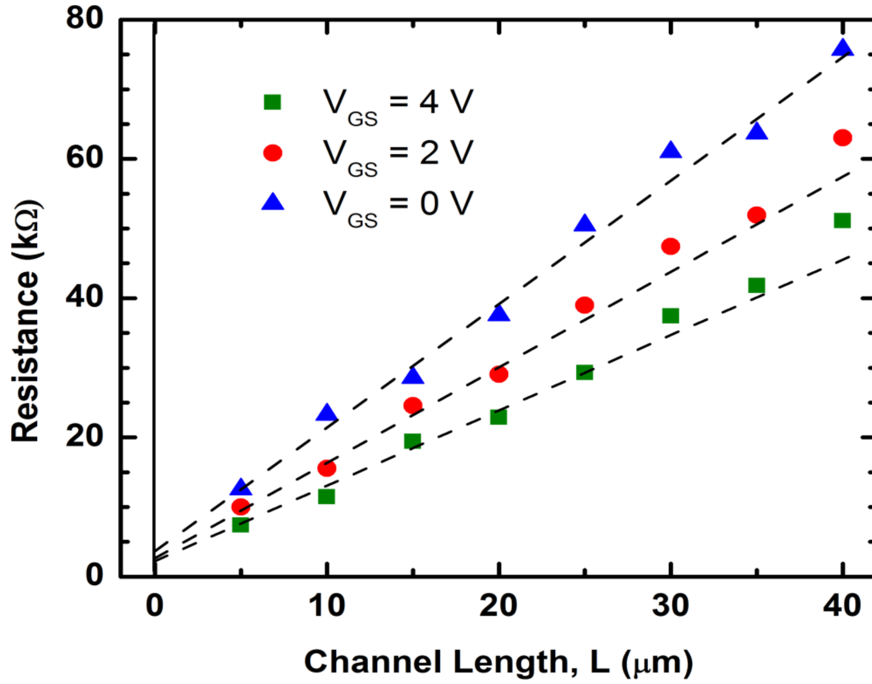

Figure 2.17: Transmission line model (TLM) measurement performed at three different gate biases to obtain the contact resistance, R_c.

The mobility in saturation under accumulation is extracted from the fit to Figure 2.16 with:

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu_{FET,sat}C_{ox}\,(V_{GS} - V_T)^2 \qquad (3)$$

from which a $\mu_{FET,sat}$ ~20-25 cm^2/V.s was obtained for V_T ~ -8.5 V, in agreement with the μ_{FET} value near pinch-off (Figure 2.19). The quadratic dependence of I_{DS} with V_{GS}, along with the low carrier velocity ~10^4 cm/s indicate that current saturation in these FET's is due to charge control and pinch off near the drain-end, as seen in long-channel MOSFET's. This is in contrast to velocity saturation seen in short channel HEMT's, which would exhibit a linear dependence of saturation current on V_{GS}. At large V_{DS}, deep in saturation, there is a region of depletion at the drain-end. However, free carriers injected from the accumulation channel near the source end are swept across the depletion region by the electric field, and the current remains nearly constant.

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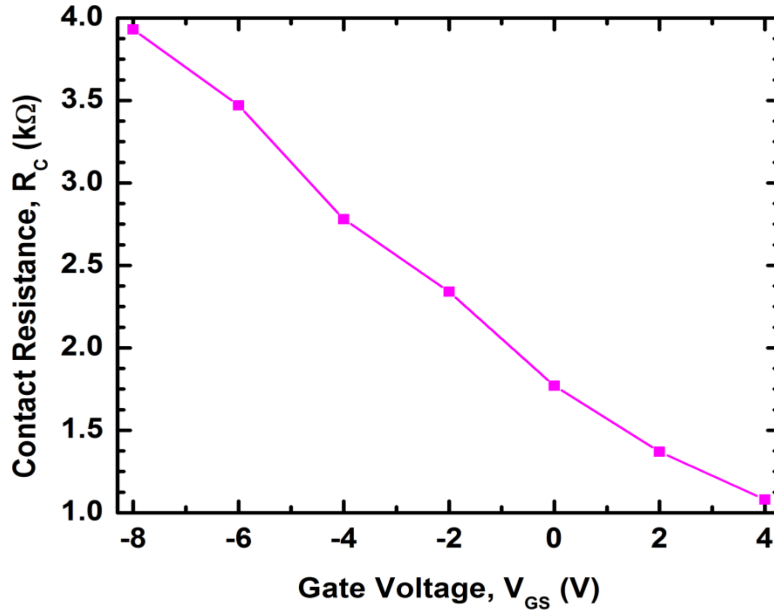

Figure 2.18: Variation of R_c as a function gate bias, measured using transmission line measurements.

The second regime of V_{GS} shown in Figure 2.16 is indicative of inversion current, i.e. hole transport as opposed to electron transport. A high degree of non-linearity is observed in the I_D-V_{DS} curves which is attributed to the large rectifying Schottky barrier (>1 eV) to the hole transport at the D-S contacts (Figure 2.20).

In Figure 2.19, we show μ_{FET} as a function of V_{GS} at V_{DS} = 0.5 V. μ_{FET} increases with V_{GS}, as the interface charges are screened by the field effect induced electrons in accumulation, increasing from ~32 $cm^2/V.s$ near depletion to ~84 $cm^2/V.s$ in accumulation with a channel carrier density of $<10^{13}$ cm^{-2}. The lowered effective mobility in saturation due to the reduced screening of charged impurity scattering at the pinched-off drain-end supports the presence of this mobility-limiting mechanism. The small increase of current with temperature is also consistent with this picture. The values of μ_{FET} at V_{DS} = 0.5 V are used to calculate sheet carrier concentration (n_s) in Figure 2.19, using $Jt = qn_s\mu E_{DS}$, where J is current density obtained from I-V measurements at V_{DS} =

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0.5 V and *t* is the average thickness of the film. Drain to source electric field is estimated to be ~50 V/cm at V_{DS} = 0.5 V.

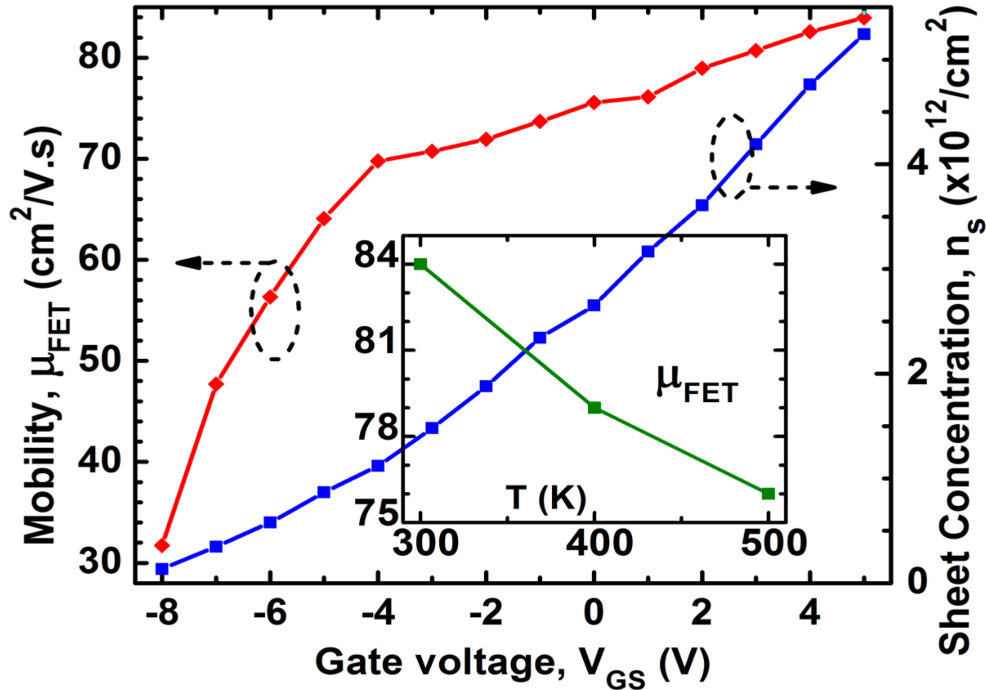

Figure 2.19: Field effect mobility (μ_{FET}) and sheet carrier concentration (n_s) as a function of V_{GS}, with inset showing the weak temperature-dependence of electron μ_{FET}.

Figure 2.20 shows the non-equilibrium energy band diagrams along the transport direction at small V_{DS} for (a) electron transport and (b) hole transport. Since the MoS_2 Fermi level is pinned to the metal Fermi level and the contacts are made of annealed Ti/Au, which forms ohmic contacts to MoS_2,[6],[19] at thermal equilibrium there is a significantly smaller barrier in the conduction band (E_C) than in the valence band (E_V). Therefore, at ON-state of the device ($V_{GS} >> V_T$), electrons are injected/extracted by the source/drain contacts very efficiently. At low V_{DS} (< 1 V), band to band tunneling (BTBT) of electrons from the drain contact to the MoS_2 E_V is unlikely due to the E_V being at a lower energy level than the drain Fermi level (Figure 2.20a), hence thermionic emission is the only mechanism of carrier injection at this regime which resulted in the maximum

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mobility of >80 $cm^2/V.s$. The situation changes when V_{GS} becomes significantly lower than V_T, and the channel experiences strong inversion; so there are two tunnel barriers seen by the holes as shown in Figure 2.20(b), which limits the hole current significantly. Although the details of the hole transport mechanism is beyond the scope of this work, we indicate the possible hole transport mechanisms as (1) thermionic emission (low probability due to very high barriers), (2) intra-band hole tunneling at the both ends of the channel and (3) band-to-band tunneling at the drain end. The highly non-linear behavior of the I_D-V_{DS} curves at inversion (Figure 2.16) also indicates the tunneling based mechanisms to dominate in this regime, as seen by others.[20],[21] This asymmetrical transport behavior may be useful in developing CMOS TFT circuits using MoS_2 FETs, where choosing the right metal contacts could enhance the transport of either type of carrier while suppressing the other one, leading to greater voltage discrimination between logic states.

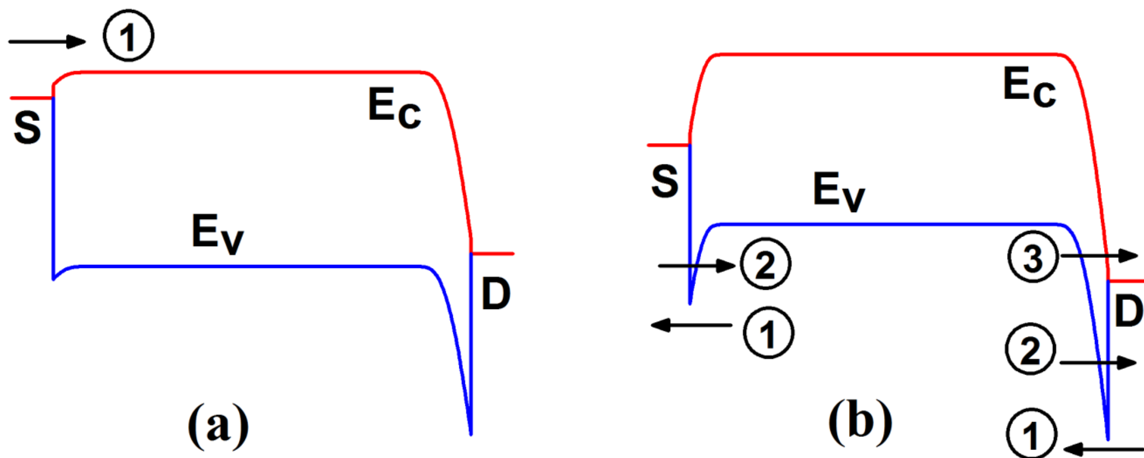

Figure 2.20: (a) Energy band diagram of the MoS_2 FET at low V_{DS}. At $V_{GS}>>V_T$, thermionic emission (1) is the dominant mechanism of electron injection in the channel, which is facilitated by the low metal-semiconductor barriers at both ends of the channel by the accumulation of electrons in the channel. (b) At $V_{GS} << V_T$, there are several possible mechanisms for hole transport in the valence band: (1) thermionic emission, (2) intra-band hole tunneling at both ends of the channel and (3) band-to-band tunneling at the drain end.

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Table 2.1 compares our FET metrics with those of other MoS_2 devices reported in the literature, including small area and large area devices, most of which required a transfer to a fresh substrate. It can be seen that our devices represent the state-of-the-art on SiO_2 dielectrics in air, with the advantage of a transfer-free process, which is highly desirable for high throughput processing with high yield.

Table 2.1 Comparison of device parameters with other works on exfoliated and synthetic MoS_2.

Work	Thickness	Method of preparation	Gate	Dielectric	μ (300 K) cm^2/V.s	n_s (cm^{-2})	SS (mV/dec)	On/Off
This work	**3-5 ML**	**CVD-Mo***	**BG**	**SiO_2**	**> 80**	**<10^{13}**	**84**	**10^5**
Kim et. al. [19]	20-80 nm	exfoliated	BG	Al_2O_3	100	(N_D) 10^{16} cm^{-3}	80	10^6
Chen et. al.[6]	ML-12nm	exfoliated	BG	BN/SiO_2	90-250	10^{11}-10^{13}	-	-
Radisavljevic et. al.[22]	ML	exfoliated	TG	HfO_2	55	-	74	10^8
Fiori et. al.[18]	few-ML	exfoliated	BG	SiO_2	23-26	2-5×10^{12}	850	10^5
Lin et. al.[23]	ML	exfoliated	TG	polymer	150	-	~ 60	10^6
Zhang et. al.[24]	ML	CVD-MoO_3	BG	SiO_2	0.23	-	-	10^5
Zhan et. al.[25]	ML-few ML	CVD-Mo	BG	SiO_2	0.04	-	-	-
Lie et. al.[26]	ML-few ML	CVD-$(NH_4)_2MoS_4$	BG	SiO_2	<10	-	-	10^5
Laskar et. al.[26]	ML-few ML	CVD-Mo**	-	-	<10	(N_D) 3×10^{20} cm^{-3}	-	-
Schmidt et. al.[8]	ML	CVD-MoO_3	BG	SiO_2	45	7×10^{12}	-	>10^6
Lee et. al. [9]	ML	CVD-MoO_3*	BG	SiO_2	0.02	-	-	>10^3
Lin et. al.[28]	2-3 ML	CVD-MoO_3	BG	SiO_2	0.8	-	-	10^5

*does not involve transfer. **does not involve transfer, grown on sapphire.

In summary, we have demonstrated an improved growth technique for synthesizing top-down, large area, transfer-free 3-5 ML thick MoS_2 on SiO_2, reducing gate leakage by >10^8 compared to a longer duration, direct sulfidation method shown in this work. FETs fabricated from these layers were characterized in accumulation, depletion and inversion modes to study the complete transfer behavior, which showed a normally-on accumulation mode characteristics with μ_{FET} > 80 cm^2/Vs, SS < 90

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mV/decade, and ON/OFF ratio of >10^5. The observed temperature stability of FET metrics up to 500 K is due to canceling of ionized impurity scattering and phonon scattering. Asymmetry was observed between the accumulation and inversion modes, which were attributed to the metal/semiconductor Schottky junctions at the source/drain ends.

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Chapter 3

Graphene and MoS_2 based Heterojunctions

In the past decade graphene has been one of the most studied materials for several unique and excellent properties. Due to its two dimensional nature, physical and chemical properties and ease of manipulation, graphene offers the possibility of integration with the existing semiconductor technology for next-generation electronic and sensing devices. In this context, the understanding of the graphene/semiconductor interface is of great importance since it can constitute a versatile standalone device as well as the building-block of more advanced electronic systems. Since graphene was brought to the attention of the scientific community in 2004, the device research has been focused on the more complex graphene transistors, while the graphene/semiconductor junction, despite its importance, has started to be the subject of systematic investigation only recently. As a result, a thorough understanding of the physics and the potentialities of this device is still missing. The studies of the past few years have demonstrated that graphene can form junctions with 3D or 2D semiconducting materials which have rectifying characteristics and behave as excellent Schottky diodes. The main novelty of these devices is the tunable Schottky barrier height, a feature which makes the graphene/semiconductor junction a great platform for the study of interface transport mechanisms as well as for applications in photo-detection, high-speed communications, solar cells, chemical and biological sensing, etc. In this chapter, we review some examples of potential applications of the graphene/semiconductor junctions.

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The literature review presented in this chapter is abridged and adopted from the review article of A. Di Bartolomeo.[1]

3.1 Applications of graphene/semiconductor Schottky diodes: Review

3.1.1 **Photodetection**

A general overview of state-of-the-art photodetectors based on graphene (and other two-dimensional materials) was recently published by Koppens et al.[2]. Here we solely focus on photodetectors based on the graphene/semiconductor junction.

G/S (graphene/semiconductor) Schottky diodes, when operated under reverse bias, can be used as photodetectors. In these devices, optical absorption takes place mainly in the semiconductor, and graphene (which is the exposed side of the junction) acts as optically transparent and anti-reflecting carrier collector. Absorption in graphene may become important at lower energies, e.g. for *IR* radiation.

Devices made of graphene as optical absorber, metal–graphene–metal (MGM) or FET structures are highly appealing for ultrafast applications, but they suffer from the limitations of the weak absorption (A≈2.3) and the short recombination lifetime of photogenerated carriers in graphene in the order of ps[3,4] and the small effective photodetection area. These limitations result in low quantum efficiency and photocurrent responsivity, which in absence of a gain mechanism, remains limited to few tens mA/W (10-20mA/W in the wavelength range $400\,nm \leqslant \lambda \leqslant 1550nm$)[5-13]. In MGM devices, photo-generated carriers are captured by the electric field of the graphene–metal contacts, so only the small fraction of carriers generated very close to the contacts can be collected by the external circuit, while the rest of the carriers generated in graphene quickly recombines without any contribution to the external photocurrent. As a result, the

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effective photo detection area in MGM detectors is restricted to narrow regions adjacent to the graphene–metal interface. G/S Schottky diodes can effectively address these issues and produce a higher responsivity with the further benefit of a semiconductor compatible technology. In GSJs (graphene/semiconductor junctions), light is absorbed in the thicker depletion layer of the semiconductor and the effective photo detection area is only restricted by the G/S contact area. The separation and transport of photo-generated carriers happen in the depletion layer of the semiconductor; if the photogenerated carriers are able to reach the graphene, they will contribute to the photocurrent, independently of their excitation location along the sensible area and without the issue of the rapid e–h pair recombination in graphene. The important point here is that once photogenerated carriers are injected into graphene by the built-in electric field, these carriers can survive much longer than intrinsically photoexcited pairs in graphene. Their lifetime is related to the probability of being back injected into the semiconductor. Furthermore, if the semiconductor has a slow intrinsic recombination time, this can further reduce the recombination rate. As results the lifetime of carriers photogenerated at the G/S junction can be several order of magnitude higher (up to milliseconds) than the lifetime in graphene. Consequently, G/S Schottky junctions can have a higher quantum efficiency that MGM devices; the external quantum efficiency is in the range of 50% and 65% depending on the wavelength. Actually, as we will discuss in this section, GSJ can even have an intrinsic gain mechanism resulting in giant responsivity. Another important and unique feature of the GSJ is that responsivity can be tuned by the applied reverse voltage bias which makes these devices an ideal platform for fast and sensitive photodetection at variable brightness.

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An extensive study on the photodetection properties of the G/n-Si Schottky junction was performed by X. An and coworkers[14] who investigated devices with CVD-grown monolayer and few-layer graphene on lightly doped n-Si (Figure 3.1(a)), built with a scalable and CMOS-compatible fabrication process. In the dark or under low power illumination (less than few μW), the I–V characteristics of the junction follow the conventional photodiode behavior, as shown in Figure 3.1(b), while at higher power some anomalies are observed (Figure 3.1(c)). From detailed measurements of the Schottky barrier heights made using graphene, doped graphene and Ti/Au on Si, the Fermi level of the substrate was found pinned to the charge-neutrality level by its own surface states, with a Schottky barrier height $\Phi_B \approx 0.8$eV. Figure 3.1(d) shows the energy band diagram at thermal equilibrium and in dark condition. Here graphene is assumed neutral and the Fermi levels of graphene and n-Si are denoted as E_F and E_{FS}, respectively. Incident photons generate e–h pairs in Si. In steady state, these excess carriers can be accounted for by introducing quasi-Fermi levels, separately for holes and electrons, near the valence and conduction band edges.

X. An et al.[14] demonstrated devices with high photovoltage responsivity R_V exceeding 10^7 V/W at low power (~10 nW). This very high responsivity renders G/Si Schottky diodes competitive devices for weak signal detection. At the lowest power of 10 nW, a $NEP \sim 1$pW/Hz$^{0.5}$ was measured, confirming the low detection limit of these devices (a power as low as 1 pW can be detected above the noise level, when integrated over 0.5 s). The corresponding detectivity was $D^* = 7.69 \times 10^9$ Jones. To further characterize the sensitivity of the device to small changes of incident power, the photovoltage responsivity (or contrast sensitivity defined as dV_{ph}/dP_{in}) was used, largely

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resulting independent of the device area and with the remarkable value of 10^6 V/W at low light intensities. In the photocurrent mode, at a given negative bias (−2 V), the response was found to remain linear over at least six decades of incident power, with a photocurrent responsivity up to 225 mA/W, which is at least 1–2 orders of magnitude higher than that reported for Ge or Si photodetectors[15,16]. The time required to switch, when the incident light is turned on or off, was a few milliseconds, which is quite appealing for applications such as high speed photography, videography, etc. The measured maximum quantum efficiency was *EQE* ~ 57% over at least 4 order of magnitude of the incident power (10^{-3} to 1 mW).

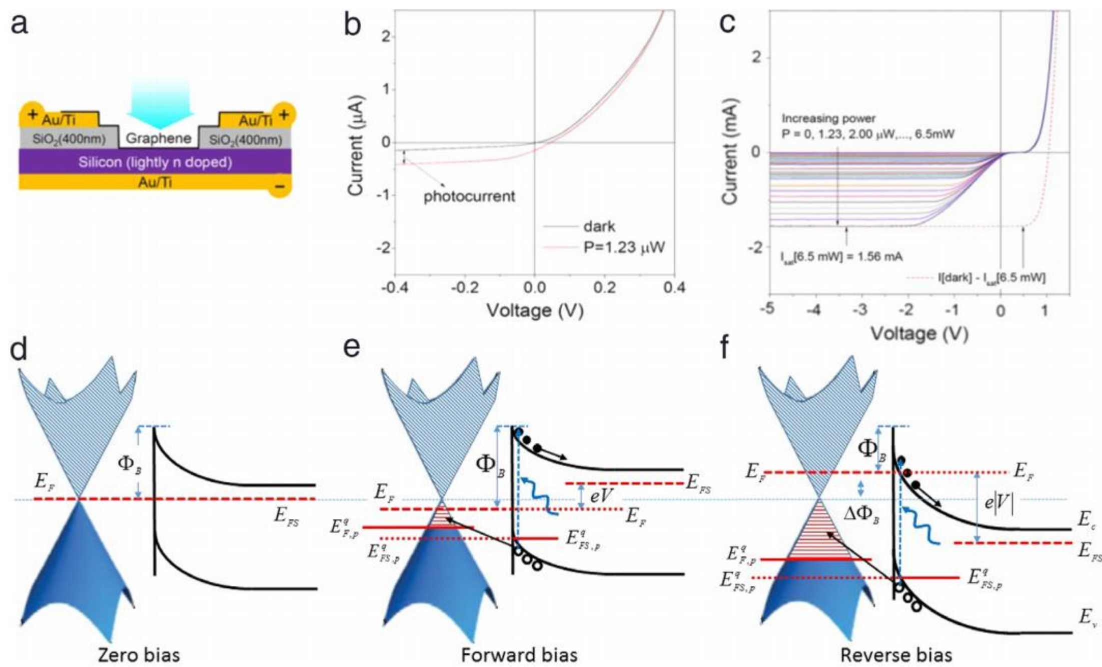

Figure 3.1: Schematic of the monolayer G/Si junction device of Ref. [14]. (b) I–VI–V curves of the device under darkness and weak illumination (P=1.23μW, λ=488nm) showing a conventional photodiode-like behavior. (c) Deviation of the I–V curves from a conventional photodiode response as the incident light power is increased up to P=6.5mW (the red dashed line corresponds to the expected behavior of a conventional M/S diode). (d) Thermal equilibrium energy band diagram in darkness (the Fermi level of n-Si is pinned to the charge neutrality level of its own surface states and $\Phi_B \approx 0.8$eV). Band diagrams and Fermi level E_F in darkness (dashed line), and quasi-Fermi level at high irradiation power under (e) forward and (f) reverse bias (the subscript S is used for silicon).

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F. Liu and S. Kar[17] recently demonstrated that devices similar to those of Ref. [14] can operate with ultra-high responsivity, up to 10^7 A/W, also in current mode. The devices, when operated in a "horizontal" (or high gain) configuration (see inset of Figure 3.2(a)) rather than in vertical photodiode mode (see inset of Figure 3.2(b)), are capable of an internal gain mechanism which they call Quantum Carrier Reinvestment (QCR). The QCR exploits the ultrafast transition of photogenerated carriers within graphene and the relatively large recombination time scale in the G/Si system, which can exceed a millisecond, to achieve ultrahigh quantum gain values. F. Liu and S. Kar[17] achieved quantum gains greater than 10^6 electrons per incident photon and responsivities approaching $\sim 10^7$ A/W.

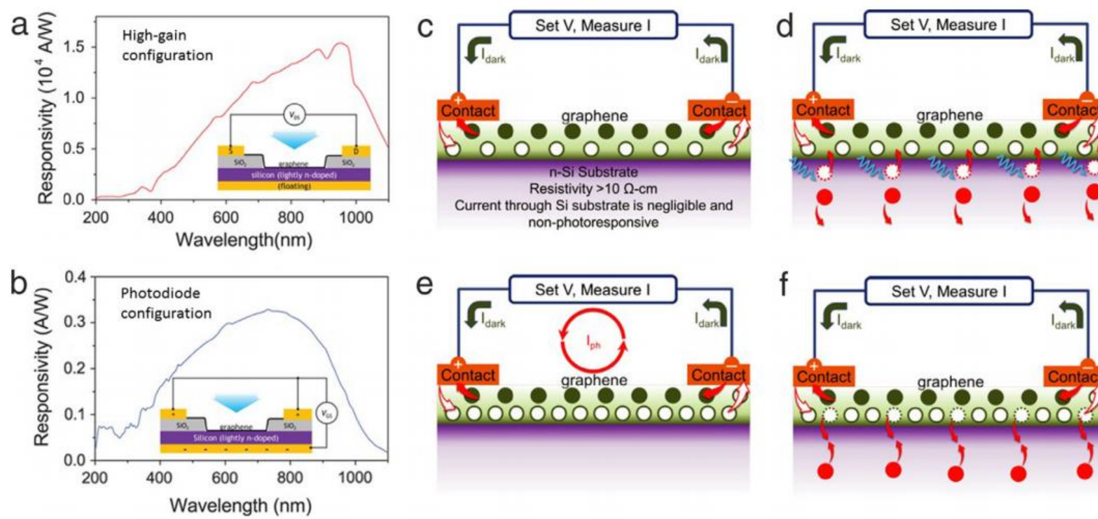

Figure 3.2: Spectral responsivity of the device (shown in the inset) of Ref. [14,17] in (a) high-gain mode and (b) photodiode mode. A dramatic difference in their magnitudes is observed, even though the spectral shapes are similar. (c)–(e) Schematics outlining the gain mechanism at the G/Si junction. Electrons and holes are denoted by dark and light circles, respectively. In (c) the dark current I_{dark} is due to intrinsic carriers in graphene. (d) Incident photons generate e–h pairs in the (lightly n-doped) silicon. Holes are swept into graphene by the built-in electric field of the junction and contribute to the current in the external circuit. Due to the fast transit time of graphene and the low probability of back injection in silicon, a single injected photocarrier can circulate several times (e) and substantially contribute to the current before recombine (f). This mechanism generate an internal quantum gain.

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Figure 3.2(a) and (b) compare the responsivity of the same device when operated in high gain mode (a) and in photodiode mode (b). As we have already pointed out, the intrinsic photocurrent in graphene is limited to a few mA/W, while the photocurrent responsivity seen in Figure 3.2(a) is many order of magnitude higher. This implies that the photocurrent of the device under study (no matter the configuration) has insignificant contributions from photocarriers generated in graphene. At the same time, the spectral shape of the responsivity curve in Figure 3.2(a) is similar to that of Figure 3.2(b), which is obtained in photodiode mode, clearly indicating that most of the photoinduced carriers originate in silicon and then get injected into graphene. The model developed to account for the far higher efficient photon-to-charge conversion in the gain-mode configuration is sketched in Figure 3.2(c)–(f). This qualitative model is based on the photoinduced injection of carriers from Si into graphene. Compared to graphene, the lightly n-doped Si is highly nonconductive and under an applied external bias V_{DS} (as in Figure 3.2(a)), and in darkness, a dark current I_{dark} flows through the external circuit due to the intrinsic carriers in graphene, as shown in Figure 3.2(c). When light is shined on the device, photogenerated e–h pairs are separated by the built-in electric field: electrons move away into the body of silicon while holes get injected across the junction into graphene, as shown in Figure 3.2(d). These additional holes, injected into graphene, add a current in graphene and in the external circuit, denoted as I_{ph} in Figure 3.2(e). Due to the extremely rapid transit of carriers within graphene, a single injected hole can "circulate" (in the sense that a hole can be removed by an electrode and replaced by a hole injected by the other electrode) many times before another "equivalent" hole reverse-injects across the junction into silicon (Figure 3.2(f)). During the lifetime of an injected hole carrier, τ_rτr, a

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time scale determined by the quantum-mechanical probability of recombination, the hole can be "reinvested" several times into the external circuit, adding to the net photocurrent, and leading to a quantum gain (QCR mechanism).

3.1.2 **IR Detection**

Graphene–Si Schottky junctions have been proposed and demonstrated also as sensitive infrared (*IR*) detectors[18]. Infrared radiation in the C band of 1528–1561 nm and the L band 1561–1620 nm is of great interest and importance for optical communications. Differently from the detection of visible light where graphene is used as a transparent electrode and photoconversion happens in the Si depletion layer, at *IR* wavelengths the photocurrent is generated in graphene.

The great advantage of the G/Si diode is that all the photo-generated carriers in graphene, independent of their excitation location, have a similar chance to be separated and transferred to Si. In fact, whenever the generated carriers pass through the thin layer of graphene, they are swept by the electric field of Si depletion layer and contribute to the photocurrent. Furthermore, the relatively short lifetime of the photo-generated carriers of graphene is not a limitation in this case because the thin graphene layer is shorter than the mean recombination length of the carriers and the photo-generated carriers in graphene in all parts of the junction have high probability to be separated at the interface with Si before recombining.

M. Amirmazlaghani et al.[18], in particular, studied the effect of 1550 nm excitation laser on I–V characteristics of an exfoliated G/p-Si Schottky junction. The reverse current of the junction (with Schottky barrier in the range 0.44–0.47 eV) increased under irradiation, corresponding to a photocurrent responsivity $R_I = I_{ph}/P_{inc} =$

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2.8−9.9 mA/W respectively at −5 V and −15 V reverse bias (the responsivity increased with reverse bias, but so did the level of noise). For comparison, all-Si detectors at the same wavelength have responsivity at least an order of magnitude lower[19].

Monolayer G/Si junctions were studied as near-infrared photodetectors also in Ref. [20], by fabricating a device able to operate at zero external voltage bias because of a strong photovoltaic behavior of the G/Si Schottky junction. A responsivity and detectivity R_I = 29 mA/W and D = 3.9×10^{11} cm.$Hz^{0.5}$/W were measured at room temperature. The device showed great potential for low light detection with intensity down to ~1 nWcm−2 at 10 K and a fast time response with speed of 100 μs, which allowed the device following a fast varied light with frequency up to 2100 Hz.

The possibility of using G/Si junctions for near to mid-infrared detection was further investigated in Ref. [21], which demonstrated the use of in-plane absorption in a graphene-monolayer structure and the feasibility of exploiting indirect transitions in G/Si junction waveguides for mid-infrared detection. A graphene/silicon photodiode was formed by integrating graphene onto a silicon optical waveguide on a silicon-on-insulator (SOI). The waveguide enabled absorption of evanescent light that propagates parallel to the graphene sheet, and resulted in a responsivity as high as R_I = 130 mA/W at 1.5 V bias for 2750 nm light at room temperature. A photocurrent dependence on bias polarity was observed and attributed to two distinct mechanisms for optical absorption, that is, direct and indirect transitions in graphene at 1550 nm and 2750 nm, respectively.

3.1.3 **Solar Cells**

The photovoltaic properties of the carbon/Si interface were initially studied with the successful formation of pp-type a-C/n-Si heterojunctions (a-C denotes a diamond-like

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amorphous carbon film) which showed efficiencies less than 1% at AM1.5[22-24]. Further development involved carbon nanotubes (CNTs)/Si junctions. The photovoltaic properties of films of CNTs on Si have been extensively studied with efficiencies varying from few percents to 14%[25-33]. Typically films of CNTs combines two types of heterostructures (Schottky and p-n), since both metallic and semiconducting nanotubes coexist in as-grown materials. A drawback of films composed of CNT networks is the interspace between bundles which reduces the conductivity of the film and the effective absorbing area, even though this can be advantageous for transparency. In this regard, graphene films are convenient since they can easily guarantee better electrical connection and full area coverage with superposing flakes.

One of the first studies on the G/n-Si Schottky junction for solar cells was reported by X. Li et al.[37] with devices consisting of a conform and continuous film of graphene sheets coated onto a patterned n-Si/SiO_2 substrate with Au contacts (Figure 3.3 (a)). Individual sheets were formed mostly by mono-layer, bilayer and few layer graphene. The graphene film served as transparent and anti-reflecting electrode for light illumination (reflection was reduced by ~70% in the visible region and ~80% in the near-*IR*) as well as active layer for e–h separation and hole transport. The built in field responsible for the photogenerated charge separation was estimated correspond to a barrier $\Phi_i = 0.55-0.75$ eV. The corresponding band-structure is shown in Figure 3.3(b). The I–V characteristics of the devices were highly rectifying (rectification ratio of 10^4–10^6) (Figure 3.3(c)) and with lnI nearly linear in the range of 0.1–0.4 V, corresponding to a diode ideality factor $\eta = 1.57$.

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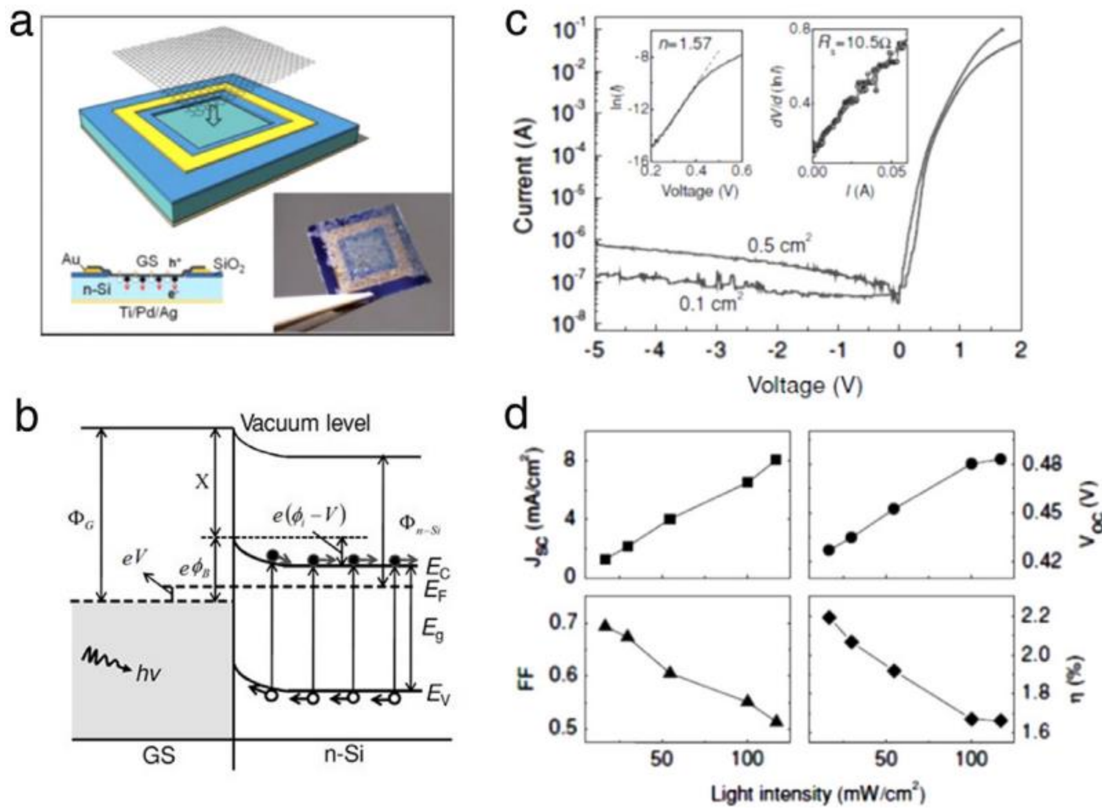

Figure 3.3: Solar cell with films of graphene on n-Si[37]. (a) Layout and a photograph of the devices. (b) Energy diagram of forward-biased G/n-Si Schottky junction upon illumination (c) I–VI–V characteristics of two devices (0.1 cm^2 and 0.5 cm^2) showing excellent rectification. The insets show the ideality factor and the series resistance of the 0.1 cm^2 cell extrapolated from the forward linear region (d) Solar cell parameters (J_{SC}, V_{OC}, *FF* and *PCE*) vs. light intensity for the 0.1 cm^2 G/n-Si cell

The reverse leakage current is nearly proportional to the area of the contact as the leakage current is restricted to the area of n-Si directly under the graphene sheet. The Schottky barrier was estimated as 0.75–0.8 eV. The photovoltaic properties of the cell were characterized at AM1.5 illumination (Figure 3.4(a)) yielding an open-circuit voltage V_{OC} = 0.42 - 0.48 V, a short-circuit current density J_{SC} = 4 - 6.5 mA cm−2 and a *FF* of 45%–56%, which corresponds to an overall PCE=1~1.7% (Figure 3.3(d)). Both V_{OC} and J_{SC} depend linearly on the light-intensity incident on the cell, consistent with a systematic increase in photogenerated carriers. The *EQE vs* photon energy is shown in Figure 3.4(b); its first derivative, displayed in the inset, presents a sharp peak around 1.2 eV, which

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corresponds to the fastest photon-to-electron conversion and can be assigned to the bandgap of silicon.

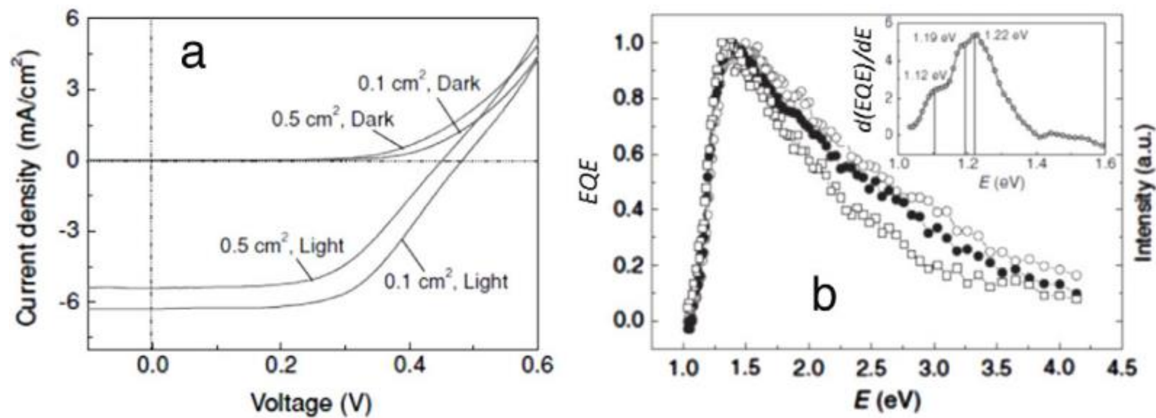

Figure 3.4: Solar cell with films of graphene on n-Si[37]. (a) J–V curves of cells illuminated at AM1.5 equivalent light (b) External quantum efficiency (*EQE*) vs. photon energy (the inset shows the differential *EQE* spectrum) for cells with different area.

The *PCE* of these devices was almost an order of magnitude lower than that reported for CNTs on Si, but it was obtained without any balancing of the conductivity and the transparency of graphene sheets and no optimization of the G/Si interface. Ref. [37] also reported the successful series and parallel combination of the cells to multiply V_{OC} and J_{SC} respectively, thus checking the feasibility of arrays of solar panels.

The photovoltaic effect of a single graphene sheet on p or n-Si was observed by C.C. Chen et al. in Ref. [34]. Solar cells were also demonstrated with graphene on CdS[35] and CdSe[36] nanowires or nanobelts, with *PCE* up to 1.65% at AM1.5.

3.1.4 **Chemical Sensors**

Graphene has an intrinsic high sensitivity for detecting chemical species. Its all-surface nature allows the ππ-conjugated system to be entirely exposed to external influences. Even the adsorption of a single molecule can affect the electronic properties of graphene, as demonstrated by Schedin et al.[38] in ultrahigh vacuum conditions.

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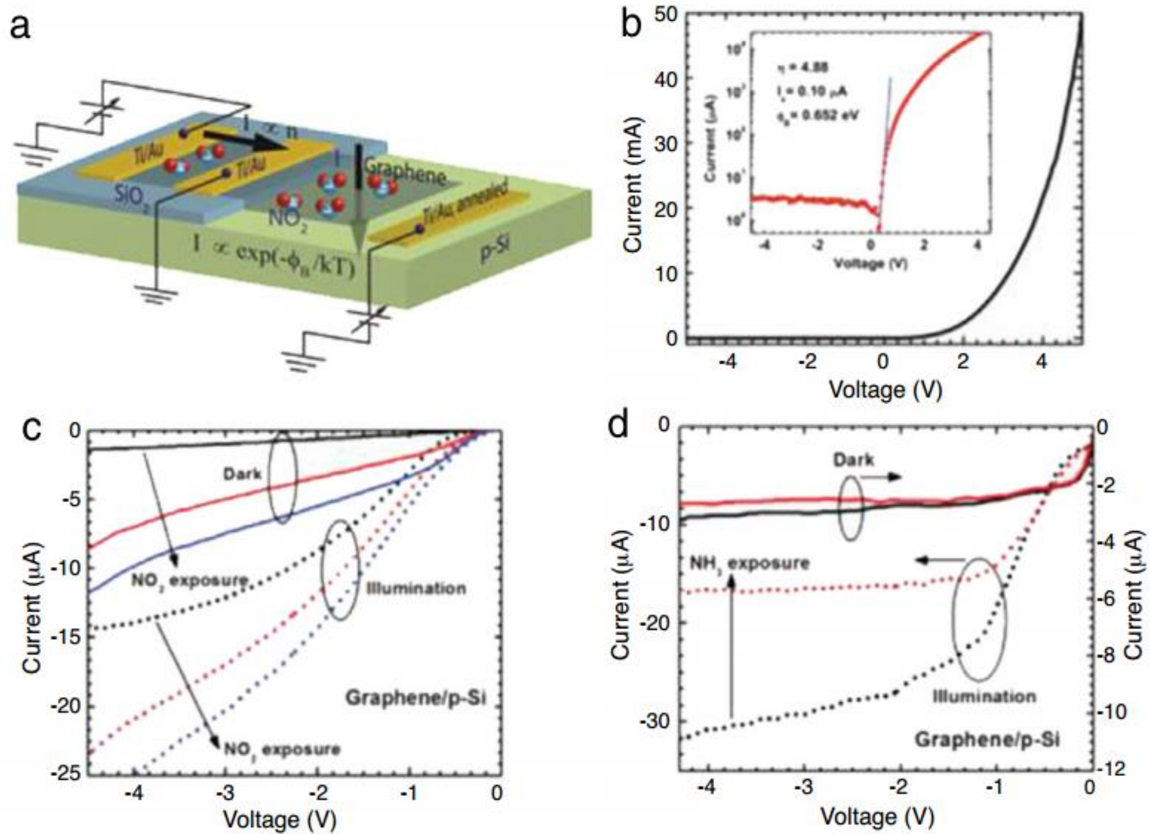

Figure 3.5: (a) Device schematic and biasing of a graphene chemiresistor and a G/Si Schottky diode sensor fabricated on the same chip[40]. (b) I–V characteristics of a G/p-Si (the positive voltage bias is applied to the Si contact). (c–d) Reverse I–V characteristics of G/p-Si diode in dark (solid curve) and under illumination (dotted curve) for different exposure times to (c) NO_2 and (d) NH_3. The black curves represent pre-exposure characteristics, while the red and blue curves represent characteristics after 10 min and 30 min of gas exposure.

H.-Y. Kim et al.[39] successfully used monolayer G/Si diodes as sensors exposing graphene to liquids and gases. These sensors showed sensitivity to liquid and gaseous electron donor (ED) and acceptor (EA) substances, such as anisole, benzene, chlorobenzene, nitrobenzene, and gaseous ammonia. The G/Si junction parameters were found to be very sensitive to the charge transfer from various adsorbates. Any change introduced by exposure was quite reversible and stable in time, two important requisites to qualify G/Si diodes as sensors.

The sensors of H.-Y. Kim et al. [39] uses the variation of the forward characteristic

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of the G/Si junction as detection principle. Some peculiarities of the G/Si junction are not fully exploited in this approach. On the other hand, using the reverse part of the G/Si Schottky junction can have the further advance of higher and bias tunable sensitivity and low power consumption, as proposed in Ref. [40]. Figure 3.5(a) shows a schematic diagram of a G/p-Si junction, which was fabricated on the same chip together with a graphene chemiresistor (a chemiresistor is a sensor based on the variation of resistance of graphene, which is inversely proportional to number of charge carriers in graphene). The I–VI–V characteristic, showing the usual rectifying behavior, is shown in Figure 3.5(b) (note that the positive voltage bias is applied to the Si contact). The reverse saturation current increases monotonically with increasing bias magnitude (Figure 3.5(c) and (d)), due to the graphene work function changes typical of G/S junction. Devices, fabricated both on p and n-substrate were exposed for different durations to dilute NH_3 (electron donor) and NO_2 gases (electron acceptor), both in dark and illuminated ambient conditions. The effect on the reverse characteristics of a G/p-Si is shown in Figure 3.5(c) and (d). With NO_2 exposure, the current increases dramatically both in dark and illuminated conditions due to lowering of the SBH (Figure 3.5(c)), while for NH_3 exposure the reduction in current is rather small in dark, but is enhanced under illumination (Figure 3.5(d)). Adsorption of NH_3 increases the SBH, thus reducing the current. However, since the current is already small, the change in current is not very large. Under illumination, the reduction in current is much more noticeable since the current is increased significantly due to excess carrier generation and barrier lowering.

The tuning the SBH and barrier width at the tiny area of contact between graphene and SnO_2 nanowires through the adsorption/desorption of gas molecules is at

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the origin of the outstanding NO_2 gas sensing properties of monolayer G/SnO_2 nanowire Schottky junction devices presented in Ref. [41]. The devices were prepared by directly growing single crystal SnO_2 nanowires on interdigitated Pt electrodes via thermal evaporation. A CVD graphene monolayer was subsequently transferred on top of the nanowire chip. The Schottky junction-based sensor showed sensitivity to NO_2 gas with the remarkable detection limits of about 0.024 ppb at the low operating temperature of 150 C and bias voltage of 1 V and with a response/recovery time of less than 50 s.

3.2 Applications of Graphene-based Barristors: Review

H. Yang et al.[42] proposed adding a top gate to the G/Si junction to control the Schottky barrier height and achieve a large modulation of the diode current (with on/off ratio up to 10^5). They fabricated three terminal devices, of the type sketched in Figure 3.6(a), which are known as graphene barristors, i.e. variable barrier devices, consisting of CVD graphene on hydrogen terminated n- or p-Si. An optimized transfer process was used to yield atomically sharp interfaces (as illustrated in the inset of Figure 3.6(b)) with minimum number of atomic defects or silicon dioxide formation to prevent charge trapping sites. The purpose was to avoid Fermi level pinning at the G/Si interface and make the graphene E_F controllable by the gate through field effect.

Figure 3.6(c) shows the I–V characteristic of a G/p-Si barristor with zero voltage on the gate, $V_{GS} = 0$ V. The ideality factor is very close to uniy, confirming the high quality of the junction. It can be noticed that, both in forward and reverse bias, the G/p-Si current is strongly modulated by the gate voltage: by stepping V_{GS} from −5 V to +5 V reduces the current by a factor that can be as high as 10^5.

The barristor works on the principle that the SBH (Figure 3.6(d)) and the current

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are modulated by the electric field of the gate[46]. The field of the gate induces holes or electrons in graphene (Figure 3.6(e) and (f)) which shift the graphene Fermi level and modify the SBH. Figure 3.6(d), referred to a G/n-Si barristor, shows that increasing V_{GS} decreases the SBH and increases the Fermi level variation in graphene. ΔE_F and the SBH are strictly correlated, $\Delta\Phi_B = -\Delta E_F$, confirming that the field-induced modulation of E_F in the absence of Fermi-level pinning is fully responsible for the variation of the SBH of the barristor. H. Yang et al.[42] also demonstrated inverter and half-adder logic circuits by developing a fabrication process of n- and p-type G/Si barristors on a 150 mm wafers with CVD transferred graphene.

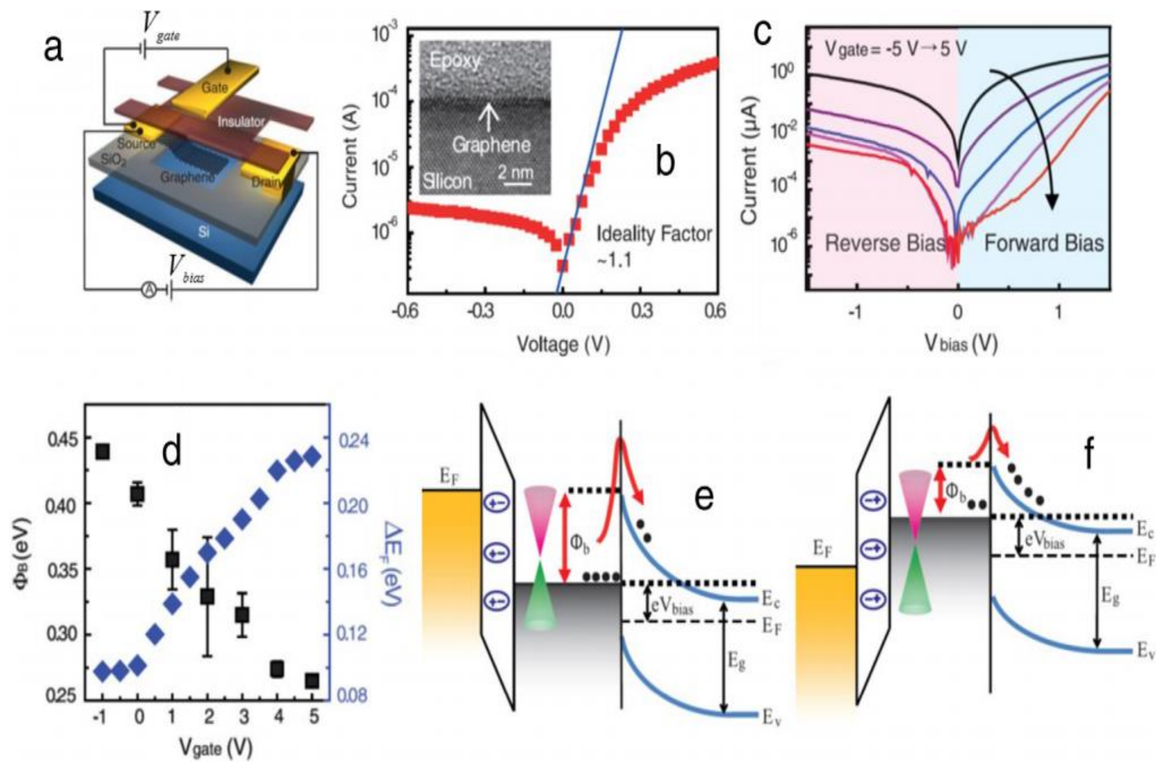

Figure 3.6: Layout of a graphene barristor with top gate[42]. (b) I–V characteristic of graphene/p-Si barristor at $V_{GS} = 0$ V. (c) I–V characteristics of the pp-type barristor for biases in the range −1.5 V to 1.5 V and gate in the range (−5,5) V by steps of 2 V. (d) SBH and field-effect induced Fermi level change, ΔE_F. (e–f) Band diagram of graphene/n-Si barristor (from left to right: gate–insulator–graphene–silicon) for (e) negative voltage on the gate (V_{gate}<0V and holes induced in graphene), and (f) positive voltage on the gate (V_{gate}>0V and electrons induced in graphene).

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M. Liu et al.[43] proposed a graphene based optical modulator for on-chip optical communications that has the advantage of compact footprint, low operation voltage and ultrafast modulation speed across a broad range of wavelengths. They fabricated a waveguide-integrated electro-absorption modulator based on monolayer graphene, which achieved modulation of the guided light at frequencies over 1 GHz. Integration of graphene with an optical waveguide greatly increased the interaction length through the coupling between the evanescent waves and graphene.

T. Gu et al.[44] used G/Si junctions as optoelectronic devices for coherent four-wave mixing. Electrophoresis was used by K. Wu and coworkers[45] to fabricate G/Si electrodes which displayed high photoresponse and high stability in aqueous solution, thus constituting solar energy materials to use in aqueous solution.

3.3 Graphene/MoS_2 Heterojunction Diodes: Review

MoS_2, which is one of the most popular TMDCs, has been thus far the most considered 2D layered semiconductor. Bulk MoS_2 has an indirect bandgap of ~1.3 eV which transforms in a direct bandgap of ~1.8 eV in single-layer form (6.5 Å thick). The direct bandgap favors interaction with light and opens the possibility of many optoelectronic applications. MoS_2 exhibits dominant n-type behavior in FET devices[47]. The electronic structure of MoS_2 also enables valley polarization, which is another important property for new-generation devices[48-50].

There are two main methods to form the heterojunction between graphene and MoS_2 (or other TMDCs). One is the mechanical transfer of exfoliated graphene onto the exfoliated MoS_2. The other is using large-area CVD-grown graphene combined with exfoliated MoS_2. Both of these methods usually need PMMA to assist in the transfer,

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even though random exfoliating method without PMMA has been sometimes used to avoid photoresist contamination and obtain cleaner interfaces. Early work was carried out mainly with the double exfoliation method, with the limitations of micrometer-scale devices and the problem of reciprocal alignment of the graphene and MoS_2. The ability to reproducibly generate large-area heterostructures with a method suitable for large scale production has been highly demanded for both fundamental investigations and technological applications. A significant progress in the fabrication was the synthesis of large-area, continuous, and uniform MoS_2 monolayers directly on graphene by chemical vapor deposition. This was reported by McCreary et al.[51], who demonstrated uniform single-layer growth of stoichiometric MoS_2 for heterostructure samples on the centimeter scale with the possibility for even larger dimensions.

Using density functional theory, Ma et al.[52] studied the geometric and electronic structures of graphene adsorption on MoS_2 monolayer to facilitate the design of devices where both the finite band-gap of MoS_2 and the high carrier mobility of graphene are needed. They found that graphene is bound to MoS_2 with a binding energy of −23 meV per C atom irrespective of adsorption arrangement and that the graphene/MoS_2 interlayer spacing is 3.32 Å, which corresponds to a weak interaction. Consequently, in this hybrid structure, the linear band dispersion relation of graphene is preserved with at most the opening of a small bandgap of 2 meV due to the variation of on-site energy induced by MoS_2. In principle, this band gap is tunable by varying the interlayer spacing, and devices combining tunable bandgap and high electron mobility become conceivable.

The energy band alignment at the G/MoS_2 interface on 3D MoS_2 single crystal was investigated in Ref. [53] where CVD grown graphene was transferred by PMMA on

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a single crystal of MoS_2. High temperature annealing (300 C) was used to remove water from the interface and obtain ultraflat CVD grown graphene as confirmed by STM images. Charge transfer between graphene and MoS_2 results in p-type doping of graphene and a downward band bending in MoS_2, corresponding to a negative space region and low charge injection barrier. Photoemission spectroscopy was used to deduce a 0.2 eV interface dipole formation (consequence of interface electron redistribution), a p-type doping of graphene corresponding to ~0.09 eV shift of the Fermi-level below the Dirac point, and a negative space charge region in bulk MoS_2 as schematized in Figure 3.7(c). Also, evidence that interlayer van der Waals interactions can modify the band structure of 2D-layered dichalcogenides was found and a ~0.1 eV MoS_2 band gap narrowing was reported.

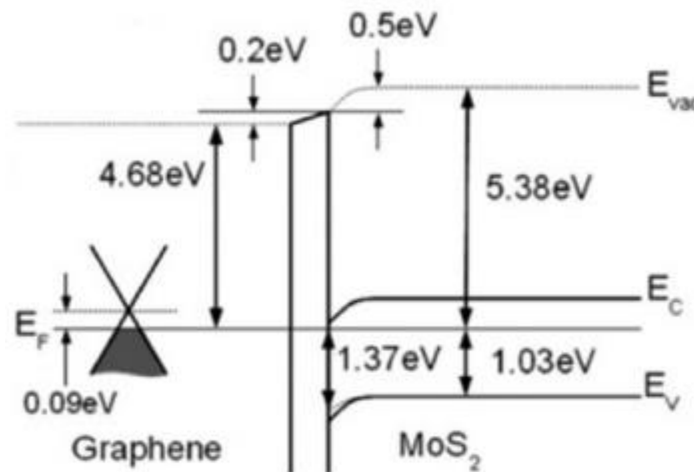

Figure 3.7: Energy band alignment at the graphene/MoS_2 interface on MoS_2 single crystal as derived from photoemission studies[53].

Yu et al.[54] have recently developed a CMOS-compatible, fully integrated process to fabricate 2D heterojunctions of graphene with monolayer MoS_2 (G/MoS_2) in large scale, based on the selective etching of 2D materials grown by chemical vapor deposition. They demonstrated high performance discrete transistors and fully integrated logic

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circuits using MoS_2 as the transistor channel and graphene as contacts and interconnects. The tunable Fermi level in graphene allows excellent work-function matching with MoS 2,such that graphene contacts on MoS_2 can yield 10 times lower contact resistance and 10 times higher on-current and field-effect mobility than conventional metal/MoS_2 contacts.

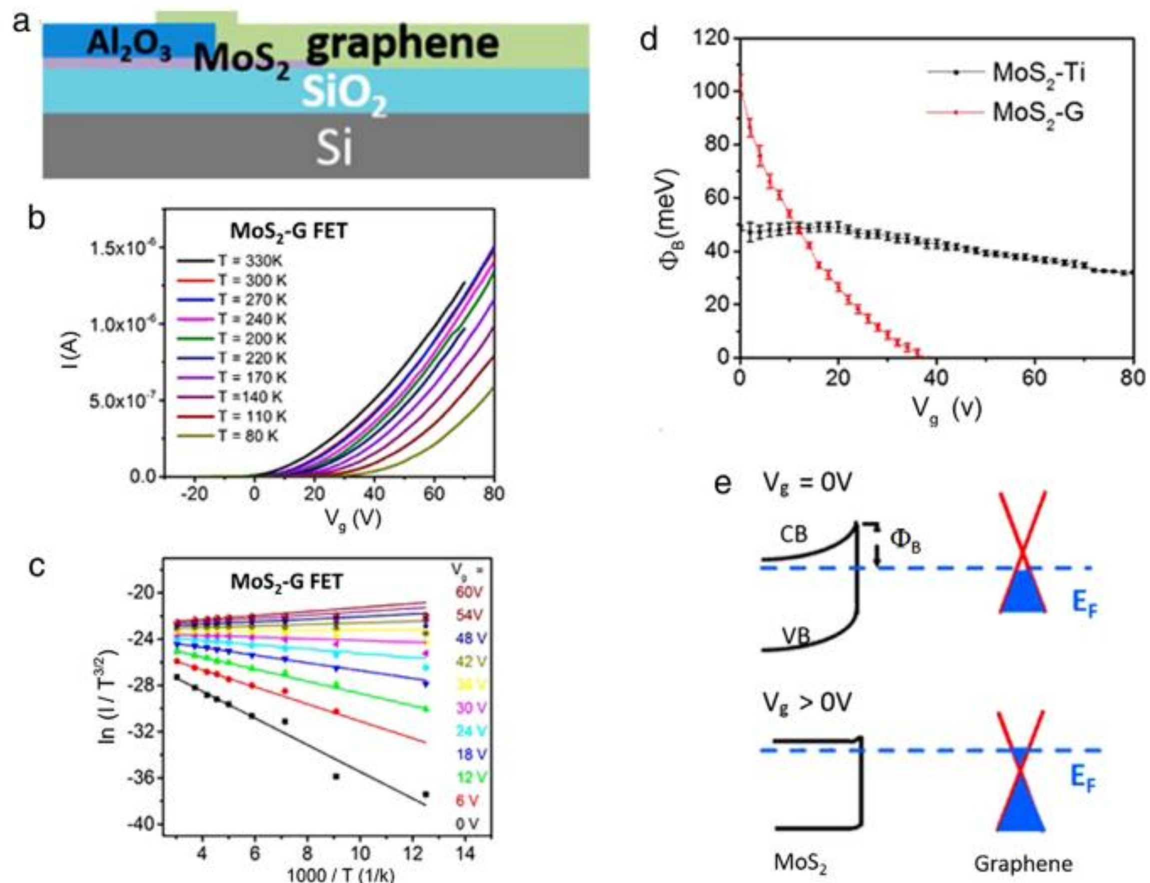

Figure 3.8: (a) Schematic of a G/MoS_2 back-gated FET (typical channel length and width are 12 μm and 20 μm)[54]. Graphene is used as source/drain contact while MoS_2 is the FET channel. (b) Source–drain current at 0.5V source–drain bias as function of the back-gate voltage V_g. (c) Richardson plot $\ln(I_d/T^{3/2})$ vs. 1000/T at different V_g. (d) Schottky barrier height as a function of the back gate bias for the G/MoS_2 and Ti/MoS_2 heterojunctions. (e) Schematic band diagram of G/MoS_2 heterostructure at $V_g = 0$ V and $V_g > 0$ V.

The device used by Yu et al.[54] is shown in Figure 3.8(a) and consists of a back-gated FET with the MoS_2 channel contacted by graphene used as source and drain, on top

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of a SiO_2/Si substrate (back-gate). Ti/MoS_2 FETs were used as control devices with exactly the same geometry.

Measurements of the current through the G/MoS_2 (or Ti/MoS_2) heterojunctions was performed at different temperatures and gate voltages V_g as shown in Figure 3.8(b). The current smoothly decreases when the temperature is lowered, indicating the presence of a small Schottky barrier at the G/MoS_2 interface. The ideality factor η and the series resistance R_s were extracted from the slope and the intercept of a plot of dV/dln(I) as a function of I, for given temperature and V_g. Reported values, at room temperature and V_g = 40 V, are η = 13.4 and R_s = 212 kΩ. R_s which corresponds to less than 0.1 kΩ·mm is ten times lower than that achieved with Ti/MoS_2 and represents a state-of-the-art contact resistance in MoS_2 device technology.

For a given V_g, the SBH of the heterojunction, Φ_B, was extracted from the slope of the straight lines in the Richardson plot of $\ln(I/T^{3/2})\ln(I/T^{3/2})$ vs. 1000/T, shown in Figure 3.8(c). Figure 3.8(d) shows the V_g-dependence of SBH for both G/MoS_2 and Ti/MoS_2 heterojunctions. The back-gate voltage has a minor effect on the SBH of Ti/MoS_2 but dramatically changes that of G/MoS_2. For G/MoS_2, Φ_B decreases from 110 to ~0 meV while V_g goes from 0 to 35 V. The modulation of the G/MoS_2 SBH is the consequence of the change in the graphene workfunction caused by the back gate. Such a change is negligible in Ti, but as we have seen many times, becomes relevant in graphene (with 300 nm SiO_2 as back gate dielectric, a change in the value of V_g by 30 V induces a change of around 200 mV in graphene work function[46]). Remarkably, when the back gate voltage is larger than 35 V, the SBH of the G/MoS_2 heterojunction approaches zero and an ohmic contact forms. The result of the SBH modulation is that graphene is capable

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to establish excellent contacts with MoS_2 and other layered semiconductors, which usually outperform those formed with traditional metals.

The tunability of the SBH by a back-gate is also exploited by Tiam et al.[55] to realize gate-controlled G-MoS_2 (and MoS_2-G-MoS_2) field effect Schottky barrier transistors (FESBTs), where the high mobility of graphene is combined with the high on/off ratio of MoS_2 transistors to overcome the low mobility of MoS_2 and the low on/off ratio of graphene FETs, respectively. Their back-gated FESBTs achieved a mobility around 60 $cm^2V^{-1}s^{-1}$ (typical values for similar MoS_2 FETs are <20 $cm^2V^{-1}s^{-1}$) and on/off ratio $>10^5$ (due to the lack of a bandgap, graphene FETs have on/off ratio <10).

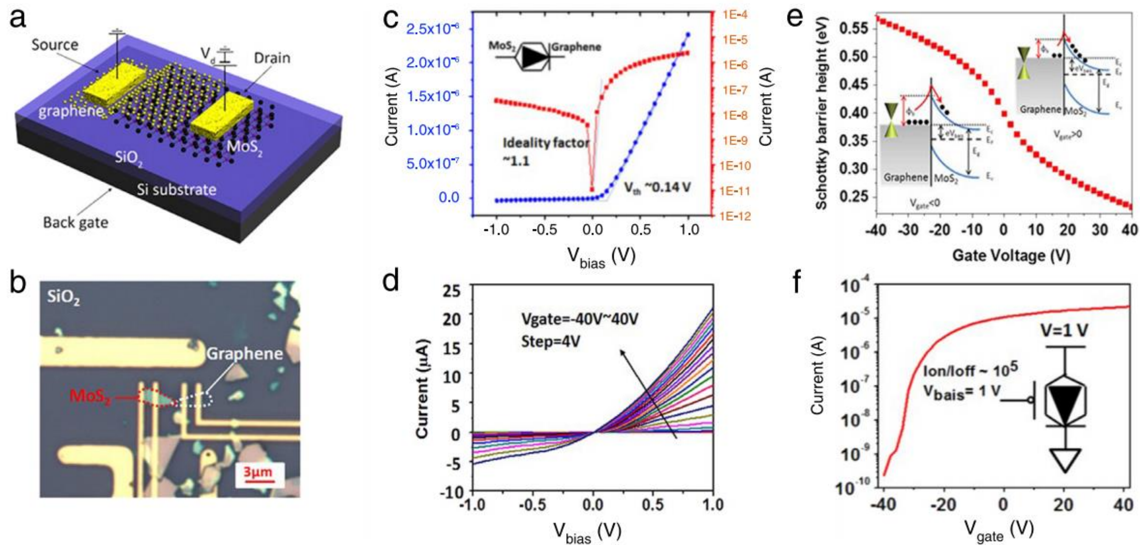

Figure 3.9: (a) Schematic of a gate controlled G/MoS_2 heterojunction[55]. The Si substrate is the back-gate, while the channel includes a G/MoS_2 heterojunction. Source and drain, respectively connected to graphene and MoS_2, are contacted by evaporated Cr/Au leads. (b) Optical image of the device in (a). The MoS_2 and graphene are ~8 nm and ~3 nm thick, the overlapping area of graphene and MoS_2 is about 1 μm^2. (c) Source–drain current vs. source drain bias (I_d–V_d) at V_g = 0 V showing rectifying behavior due to the Schottky barrier formed at the G/MoS_2 interface. (d) Output characteristics I_d–V_d at different gate biases. (e) SBH as a function of V_g at drain bias V_d = 0 V: a sweep of the gate voltage from −40 V to +40 V results in a variation of 0.34 eV of the SBH (or of the Fermi level of graphene). (f) Transfer characteristic of the G/MoS_2 FET of (a).

The schematic structure and an optical view of the G-MoS_2 heterojunction

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FESBT, fabricated with few-layers MoS_2 and graphene flakes, mechanically exfoliated onto n-Si substrates covered by 300 nm SiO_2, are shown in Figure 3.9(a) and (b). The G/MoS_2 layers form a Schottky junction which is the core part of the device and the reason of the rectifying characteristic shown in Figure 3.9(c). At $V_g = 0$ V, the source–drain current I_d shows a rapid increase at forward bias, when the source–drain voltage V_d is ramped from 0 to 1 V, with a low threshold voltage $V_{th} = 0.14$ V (see Figure 3.9(c)). The low V_{th} is desirable for low voltage applications. At $V_g = 40$ V and $V_d = 1$ V, a current density as large as 2400 A/cm^2 is obtained. Similarly to the G/MoS_2 heterojunction of Figure 3.8, the FESBT output characteristics (I_d–V_d curves) at different gate voltages V_g (Figure 3.9(d)) display a clear increase in conductance for higher V_g. As already pointed out, the change of the current flow is due to the modulation of the SBH by gate voltage, as shown in Figure 3.9(e). Finally the transfer curve in Figure 3.9(f), plotted on a log scale, shows that the FESBT exhibits a 10^5 on/off ratio and is used to estimate a carrier mobility of 58.7 cm^{2}V^{-1}s^{-1}. We notice that the ability of the gate to control the SBH and thus the transistor current can be further enhanced by replacing the gate oxide with a thinner or a higher-k one.

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Chapter 4

Graphene/MoS_2 Barristor: Electronic and Optical Characteristics

In this chapter, we demonstrate a large area MoS_2/graphene barristor, using a transfer-free method for producing MoS_2 of 3-5 monolayers (ML) thick. The source-drain diodes show good rectification, with ON/OFF~10^3. The temperature dependent back-gated study reveals the Richardson's coefficient to be 80.3±18.4 A/cm^2/K and mean electron effective mass of (0.66±0.15)m_0. Capacitance and current based measurements show the effective barrier height to vary over a large range, 0.24-0.91 eV due to incomplete field screening through the thin MoS_2. Finally we show that this barristor shows significant visible photoresponse, scaling with the Schottky barrier height. Response times of ~10s suggest that photoconductive gain is present in this device, resulting in high external quantum efficiency.

Graphene and MoS_2, 2-dimensional crystals have attention in the recent years due to their exceptional properties, such as ultra-high mobility,[1] thermal conductivity,[2] high on-off ratio and low subthreshold slope in field effect transistors,[3],[4] high photosensitivity.[5],[6] Interestingly, these two materials have certain contrasting properties, for example, graphene based FETs have poor switching performance[7] while MoS_2 based FETs can outperform many state-of-the-art ultra-low power transistors.[3][4] Fabricating a Schottky diode made of graphene and MoS_2 allows the unique properties of these two materials to be combined and has been shown to be useful.[8]-[12]

A key property of these 2D heterojunctions is that each constituent of the

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heterojunction is so thin that it may not able to completely screen an electric field from the second constituent, i.e. the Debye screening length can be greater than the layer thicknesses, so that voltage-induced interfacial tuning is achievable. This capability is unique to thin layers, most practically achieved in 2D heterojunctions,[13] and has been exploited in recent barristors,[14]-[20] which are 3-terminal devices with Schottky diodes with barrier heights tuned with a gate. Such a tunable Schottky diode, similar to a triode vacuum tube is attractive for applications in RF circuits, photodetection and chemical sensing, analog and digital electronics, etc, with all the advantages of solid state devices e.g. high speed, low-cost and compactness.[14]-[20]

In this section, we demonstrate such a graphene/MoS_2 barristor, using CVD (chemical vapor deposition)-grown graphene transferred on to as-grown pre-patterned MoS_2 thin films. Using a degenerately doped Si back gate and thermally grown SiO_2 dielectric, we successfully demonstrated the barristor functionality. By varying the gate bias between -20 V and +10 V, the barrier height can be modulated by >0.65 eV. We show the current-voltage (I-V) and capacitance-voltage (C-V) characteristics of this device are used to extract the Richardson's coefficient and electronic effective mass in MoS_2 using a thermionic emission model, from which the electrostatics of the device are elucidated.

4.1 Growth and Fabrication of the Barristor Devices

The high quality 3-5 ML (monolayers) MoS_2 samples were grown on 100 nm SiO_2/n^+-Si substrate by partial oxidation and subsequent sulfidation of Mo, as described in [21]. This method results in a pre-patterned transfer-free MoS_2 film and is not detrimental to the quality of the SiO_2 substrate. Ti/Au metal pads were fabricated on

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specific areas to serve as contacts to MoS_2 and graphene patterns, followed by a 300 ^oC annealing in forming gas. High quality 1-2 ML graphene was grown separately on high purity Cu foils using CH_4/H_2 precursor gases at around 1000 ^oC in a tube furnace, details on the growth parameters can be found in [22]-[23].

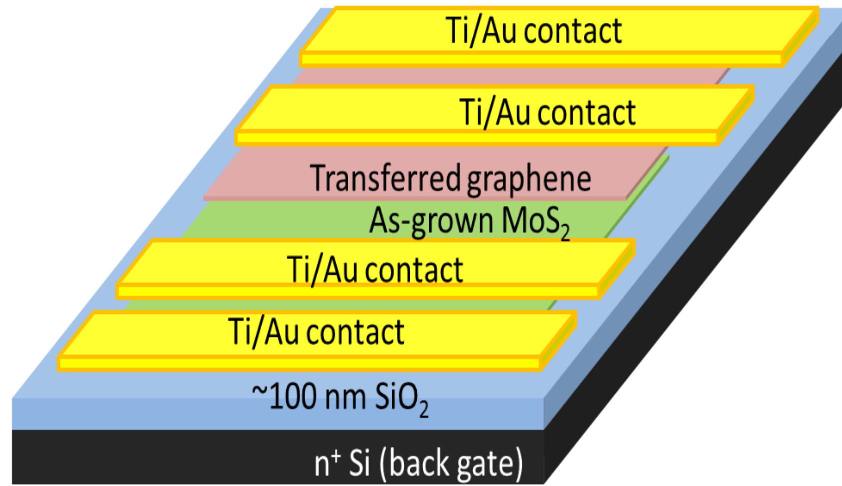

Figure 4.1: Schematic of the simultaneously fabricated MoS_2 FET, MoS_2/graphene heterojunction device and graphene FET on the same SiO_2/n^+ Si substrate.

The graphene/Cu bilayer was then coated with polymethyl meth-acrylate (PMMA) for mechanical stability, the Cu was then etched in $FeCl_3$ solution. [22]-[23] After many rinses with HCl solution and deionized water, the PMMA/graphene bilayer was then transferred on to the as-grown MoS_2/SiO_2 sample. After removing the PMMA in acetone, the graphene film was patterned using O_2 plasma in a reactive ion etching (RIE) system. A second layer of Ti/Au metallization with larger contact pads was performed on top of the annealed contacts for both MoS_2 and graphene to improve the contact resistance. Figure 4.1 and Figure 4.2 show the schematic and the optical microscopy images of the final device structure respectively, where we see that the four contacts allow measurements not only on the MoS_2/graphene heterojunction, but also on the MoS_2 and graphene films individually.

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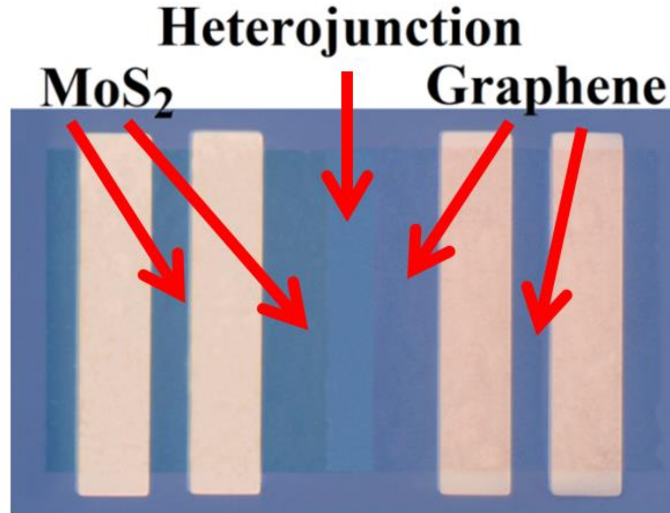

Figure 4.2: Optical microscopy image of the fabricated device showing the partially overlapping MoS_2 and graphene films with their metal contacts.

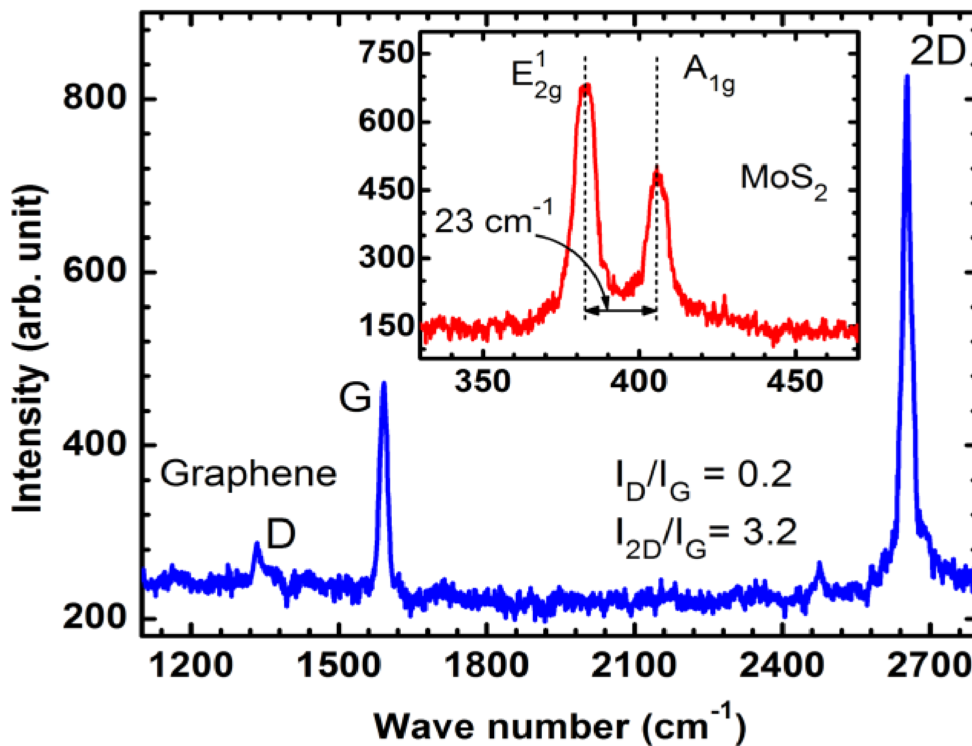

Figure 4.3: Raman spectra of graphene and (inset) MoS_2. The D, G, 2D peaks of graphene and the E^1_{2g} and A_{1g} peaks of MoS_2 are labelled.

Figure 4.3 shows the Raman spectra for graphene and MoS_2 after the final device fabrication. The ratios of peak intensities, $I_D/I_G = 0.2$ and $I_{2D}/I_G = 3.2$ indicate low defect

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density and good quality mono- or bi-layer (1-2 ML) graphene. The inset of Figure 4.3 shows the Raman spectra for MoS_2, where the characteristic peaks of E^1_{2g} and A_{1g} are observed. The separation between the peaks is about 23 cm^{-1}, which is indicative of 3-5 ML of MoS_2.[24]

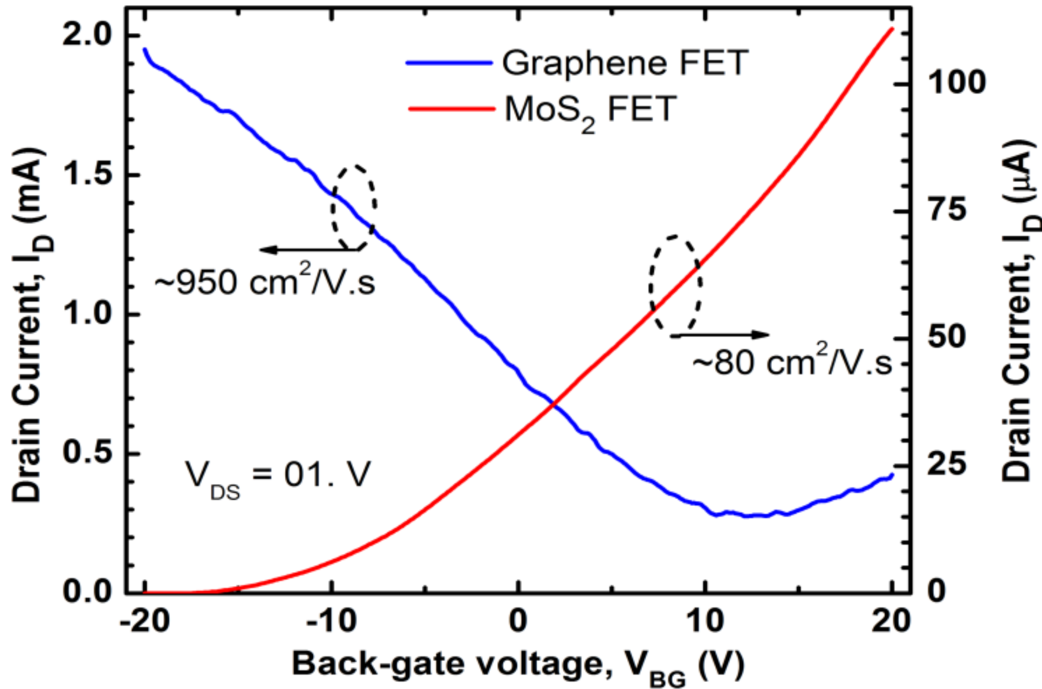

Figure 4.4: Individual transfer characteristics of the MoS_2 and graphene based FETs at 0.1 V drain bias.

4.2 Electrical Characteristics

A temperature controlled chuck and cryostat were used to study the effect of temperature on the I-V and C-V (at 100 kHz) characteristics of the devices. Figure 4.4 shows the transfer characteristics of the constituent MoS_2 and graphene field effect transistors shown, at V_{DS}= 0.1 V. These FETs were formed on the extended parts of MoS_2 and graphene layers outside of the heterojunction, and probed by the additional contacts fabricated on them (Figure 4.1). The field effect mobility of graphene was 950 cm^2/V.s, while for MoS_2 the ON-state mobility was ~80 cm^2/Vs, comparable to our

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previously reported values.[29],[25]

Figure 4.5 shows the I-V curve of the MoS_2/graphene diode structure at ~180 K temperature, where an ideality factor of 1.12 and reverse saturation current $I_0 = 2\times10^{-13}$ A are observed. The low temperature measurements were performed at the melting point of various pure solvents. The solvents were frozen by liquid nitrogen and the stable temperatures at their melting points were used for the measurements. During the low temperature measurements, a strong flow of dry ultra high purity (UHP) N_2 was used to flush the surface of the sample to avoid condensation of atmospheric moisture on the device.

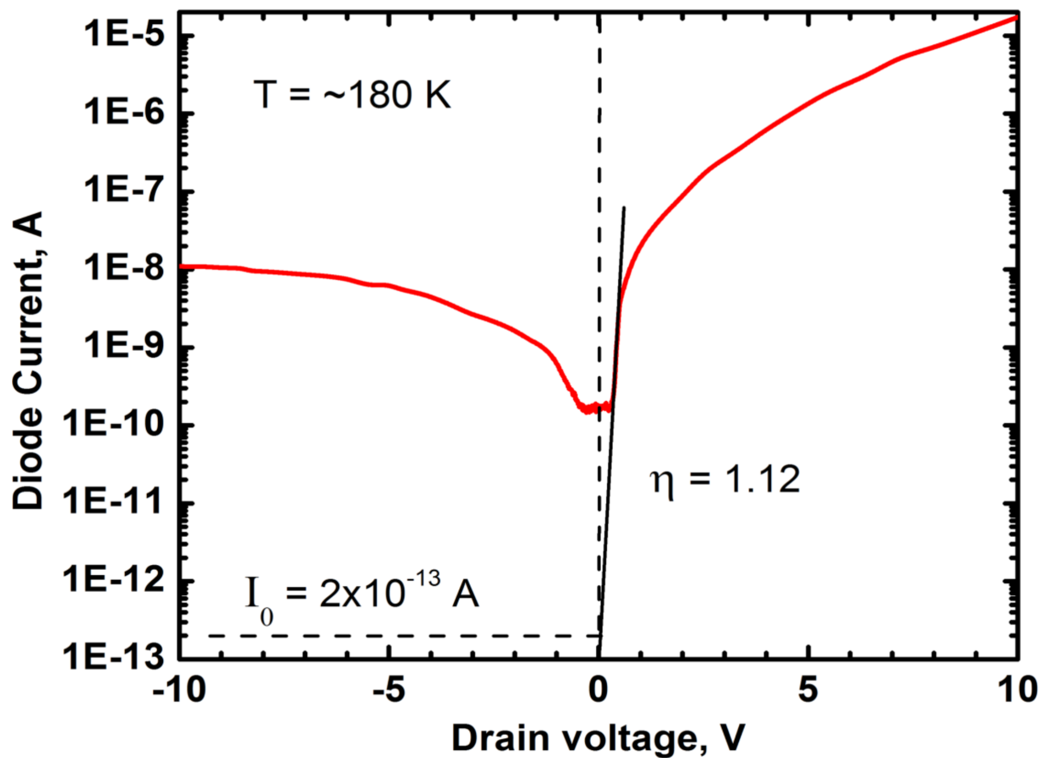

Figure 4.5: I-V characteristics of the MoS_2/graphene heterojunction at ~180 K temperature, with ideality factor of 1.12 and reverse saturation current of about 200 fA.

Figure 4.5 shows the I-V curve of the MoS_2/graphene diode structure at ~180 K temperature, where an ideality factor of 1.12 and reverse saturation current $I_0 = 2\times10^{-13}$ A

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are observed. The low temperature measurements were performed at the melting point of various pure solvents. The solvents were frozen by liquid nitrogen and the stable temperatures at their melting points were used for the measurements. During the low temperature measurements, a strong flow of dry ultra high purity (UHP) N_2 was used to flush the surface of the sample to avoid condensation of atmospheric moisture on the device.

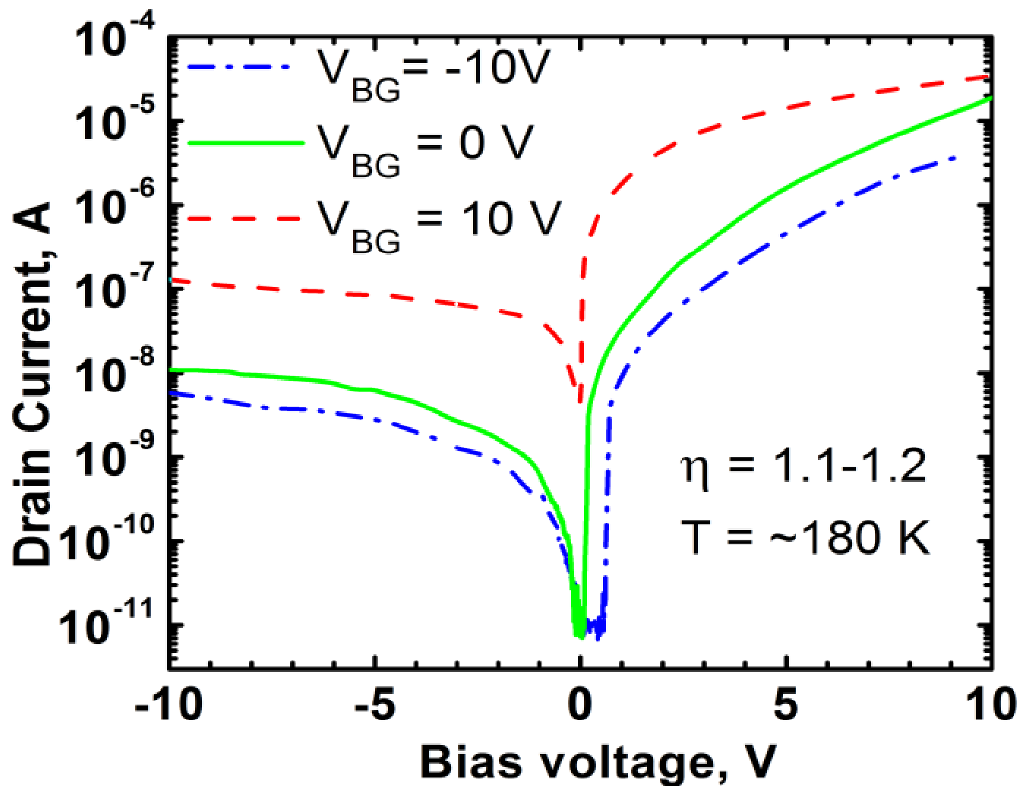

Figure 4.6: I-V curves for three different back-gate biases for the MoS_2/graphene barristor device at ~180 K (dark), with the drain contact being on graphene.

Figure 4.6 shows the I-V curves for the MoS_2/graphene barristor for three different gate voltages, the measurements were taken at ~180 K temperature in a dark environment, with graphene contact being used as the drain electrode. The current was >10^3 times lower in the reverse bias compared to the forward bias, demonstrating the clear rectifying behavior of the junction. The effective junction area of this device was

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$5\times100\ \mu m^2$, and the distance between the edge of the junction and the MoS_2/graphene contact was 5 μm. Since MoS_2 is n-doped[21] and graphene is p-doped[22] at $V_{BG} = 0$ V (Fig.1(d)), $V_{BG} < 0$ V will cause depletion in MoS_2 and accumulation in graphene, while $V_{BG} > 0$ V will do the opposite.

The current through the heterojunction is controlled by the Schottky barrier height and ideality factor at small biases. For this particular measurement, we found the ideality $\eta < 1.3$, which is reasonably good given the difficulties of forming a low-impurity interface between MoS_2 and graphene. We repeated the I-V measurements for gate voltages ranging between -20 V and +10 V, at different temperatures from 160 K to 350 K (with ±2 K accuracy). The reverse saturation current (I_0) is obtained by finding the Y-axis intercept of the log(I) vs V curves and expressed as current density, J_0. Using the thermionic emission model, we express the diode current as follows:

$$J = J_0\left[\exp\left(\frac{qV}{\eta k_B T}\right) - 1\right] \tag{4}$$

$$J_0 = A^* T^2 \exp\left(\frac{-q\Phi}{k_B T}\right) \tag{5}$$

The Richardson's coefficient (A*) is related to effective mass of electrons (m*) by:

$$A^* = 4\pi q k_B^2 m^*/h^3 \tag{6}$$

where, η is the ideality factor, k_B is the Boltzmann's constant = 1.3806×10^{-23} J/K, h is Planck's constant = 6.626×10^{-34} J.s, q is the electronic charge = 1.609×10^{-19} C, while Φ is the Schottky barrier height.

In Figure 4.7, we plot $\ln(J_0/T^2)$ vs $q/(k_BT)$, where we show the linear fit for each gate voltage, drawn through the data points for which η was less than 1.3. For V_{BG} = -10 V and -20 V, $\eta < 1.2$ even for the high temperature measurements, and all data points

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matched closely with the linear fit. However, for V_{BG} = 0 V and +10 V, the data points at higher temperature started to show saturation behavior and η started to rise above 1.3 quickly. This can be attributed to the series resistance that played a dominant role in limiting the current at its already high value, and thus significantly increasing the ideality factor. The slope of each fitted straight line indicates Φ, which is shown in Figure 4.9. Also the Y-axis intercept of these fitted lines indicate the mean Richardson's coefficient $A^* = 80.3\pm18.4$ A/cm^2/K and mean electron effective mass, $m^*/m_0 = 0.66\pm0.15$ accurately describes the transport over all temperature and V_{BG} ranges measured, supporting the starting assumption of thermionic emission ((4). These values are consistent with those previously reported for exfoliated MoS_2 based MoS_2/graphene heterojunctions, and with theory (Table 4.1).

Table 4.1 Comparison of barrier height and Richardson coefficients with other works on graphene/MoS_2 heterojunction.

Work	A^* (A/cm^2/K)	m^*/m_0	Φ (eV)	MoS2 preparation	Oxide/ Substrate
This work	80.30±18.4	0.66±0.15	0.24-0.91	CVD	SiO_2
Tian et. al.[8]	-	-	0.23-0.57	exfoliated	SiO_2
Kwak et. al.[9]	-	-	0.23	exfoliated	SiO_2
Peelaers et. al.[26]	45.86-117.07**	0.38-0.97	-	theoretical	-
Yu et. al.[27]	56.72**	0.47	-	theoretical	-

** Calculated from m* using (6).

We also performed C-V measurements to estimate the Schottky barrier height between graphene and MoS_2, and the carrier concentration of MoS_2. The back-gate was used to modulate both parameters to demonstrate the barristor action, and the $1/C^2$ vs reverse bias (MoS_2 contact used as the drain) plots are shown in Figure 4.8. We see that

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the $1/C^2$ vs V plots are linear at the low bias ranges, which allows us to fit the curves to the following equation for an n-Schottky junction:

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_{MoS2}n}(\Phi - V) \quad (7)$$

where, ε_{MoS2} = dielectric permittivity of MoS_2,[28] n = MoS_2 carrier concentration. Here we showed the effect of illumination as well, which have a significant effect on the barristor, and will be discussed shortly. Using ((7), we can estimate Φ and n for various back gate biases, with and without illumination.

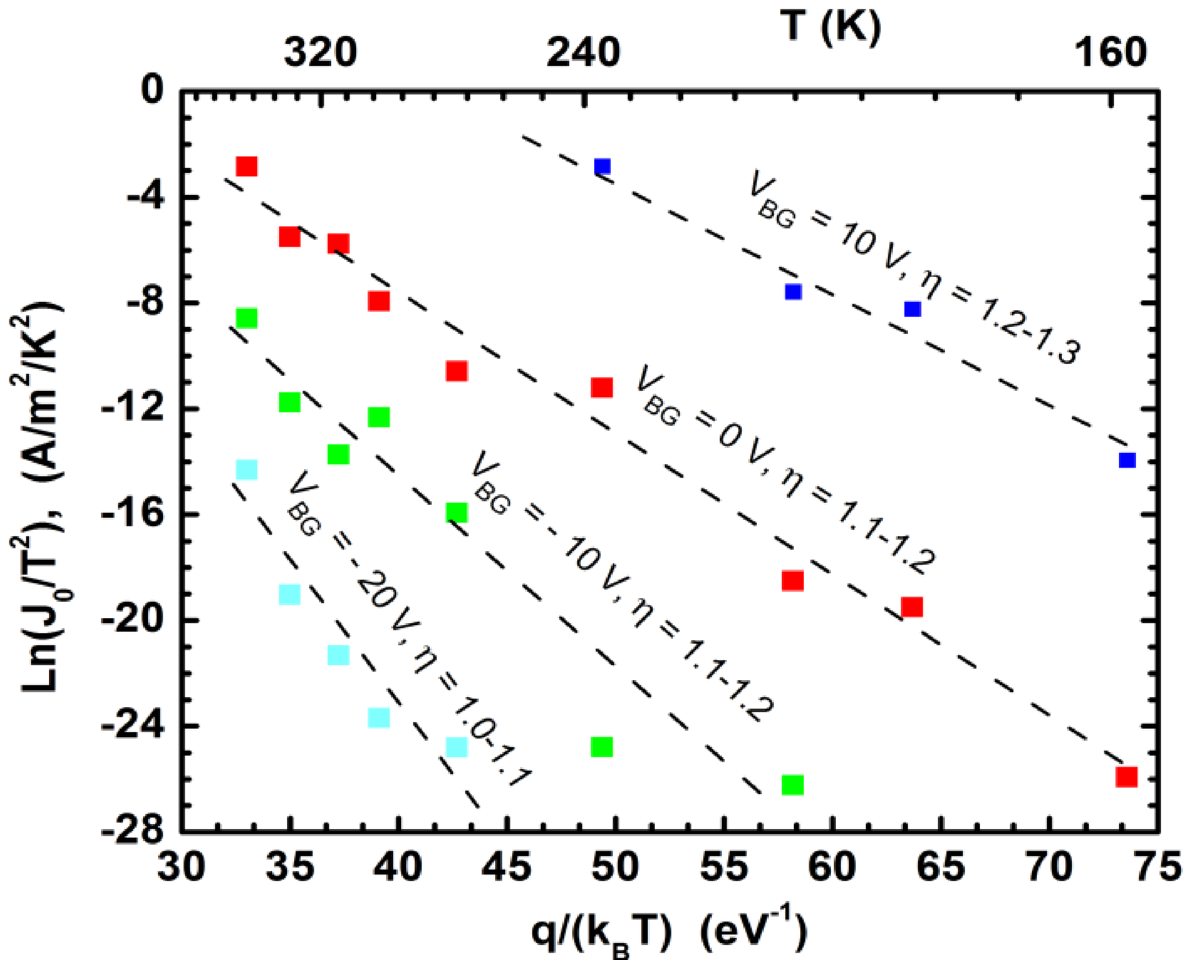

Figure 4.7: Arrhenius plots of J_0/T^2 as a function of 1/T for different back-gate biases, used for calculating effective Schottky barrier height and Richardson's coefficient for each case using thermionic emission model.

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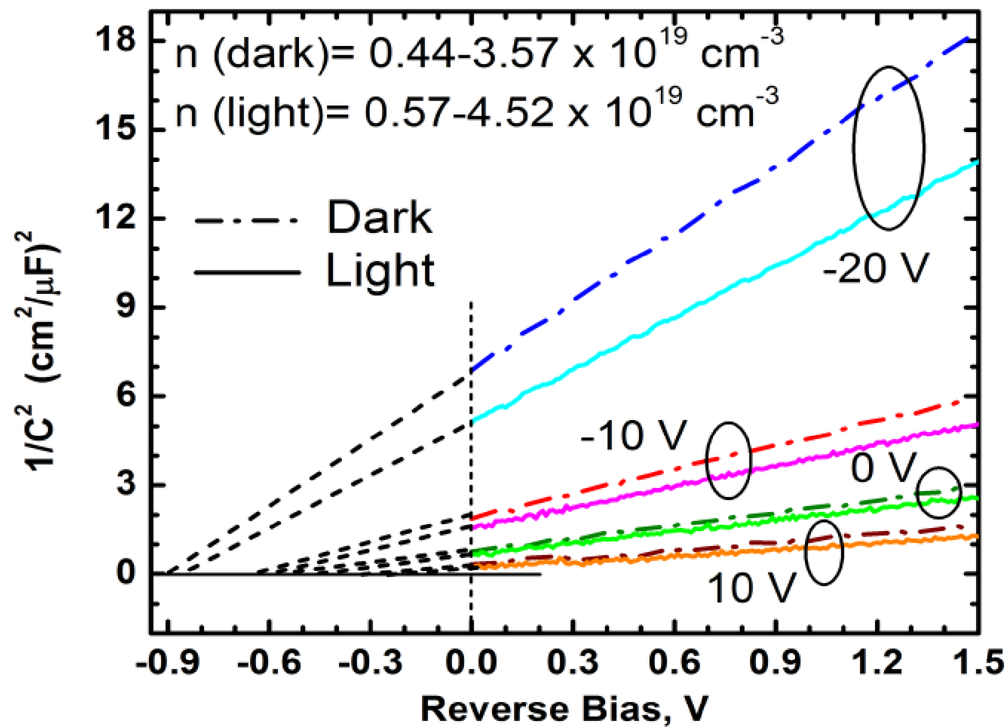

Figure 4.8: $1/C^2$ vs reverse bias for MoS_2/graphene barristor at room temperature for three different back-gate biases, with and without illumination.

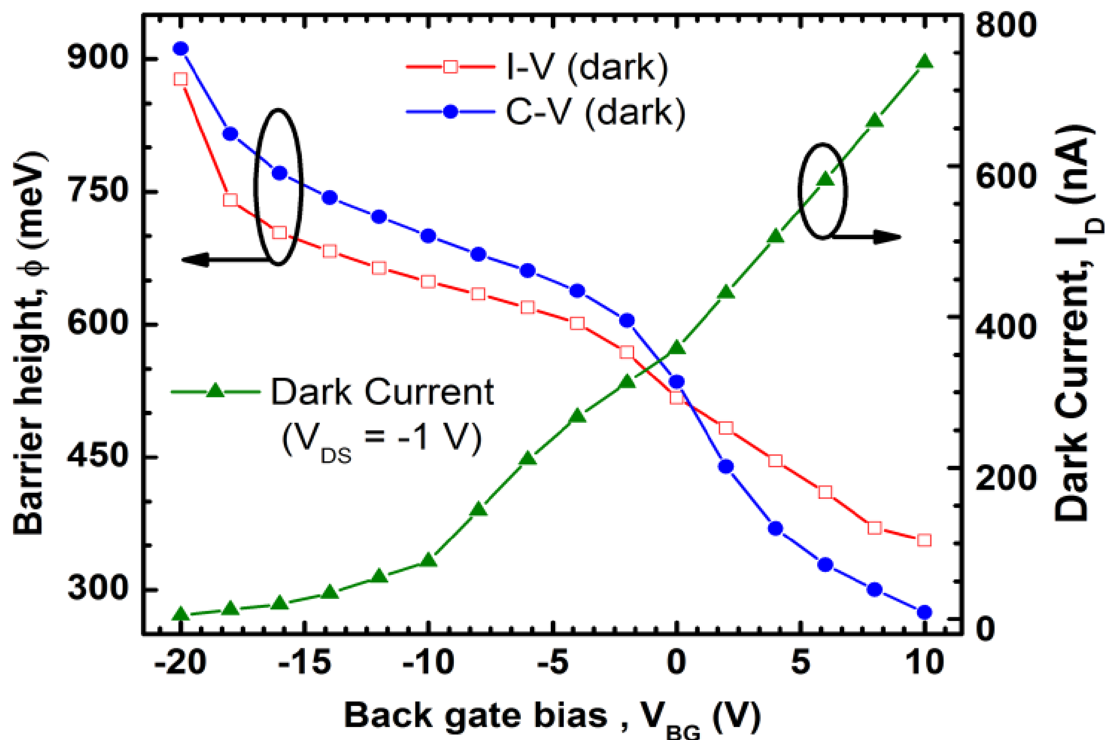

Figure 4.9: Calculated dark current at V_{DS} = -1 V and barrier heights from C-V and I-V measurements of MoS_2 without illumination for different back-gate biases.

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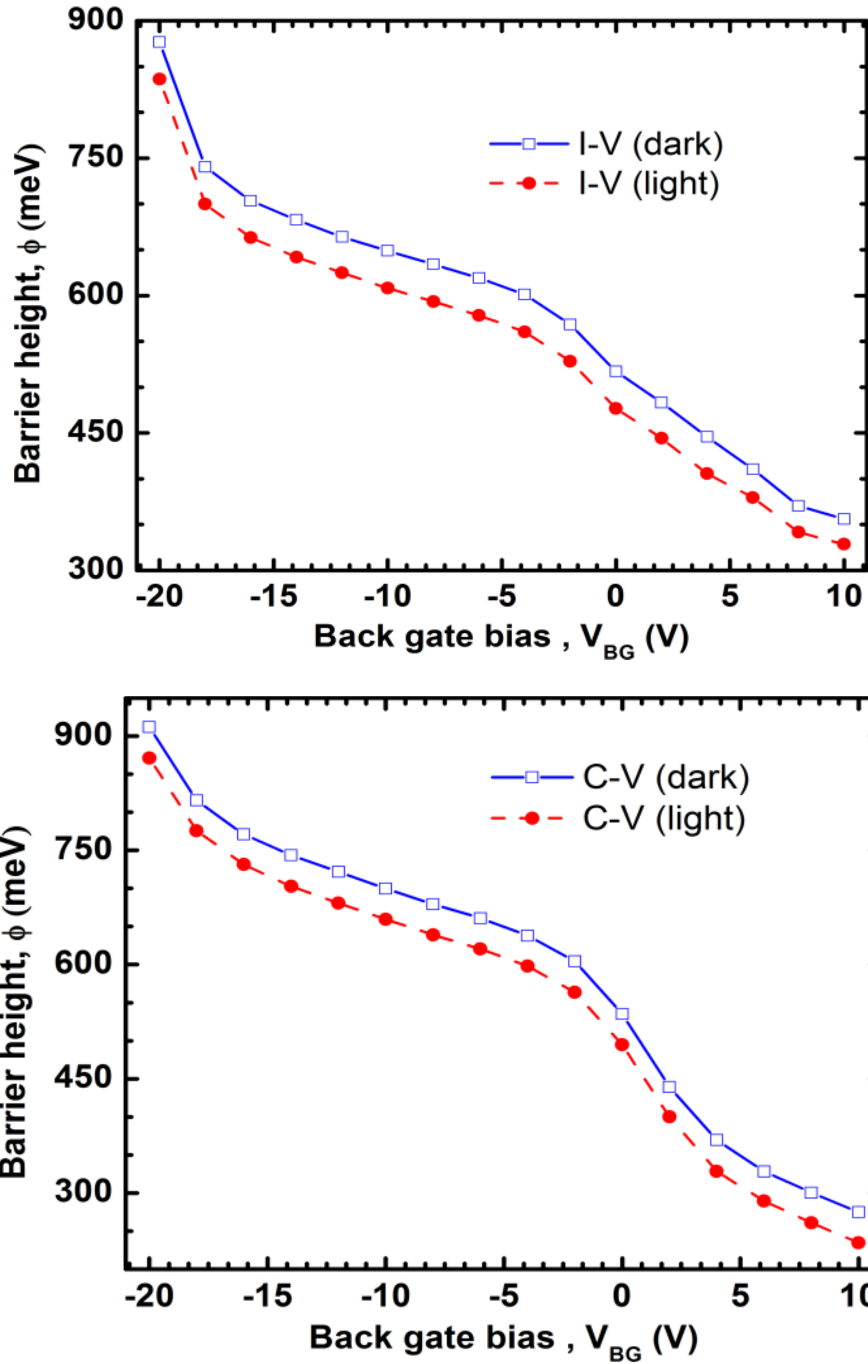

Figure 4.10: Calculated barrier heights from (top) I-V and (bottom) C-V measurements respectively, as a function of V_{BG} and presence/absence of light (10 W/m^2 optical power).

We compared the Φ obtained from C-V and I-V (thermionic emission model) measurements for gate voltages between -20 V and +10 V, and both measurement techniques revealed similar correlation between Φ and V_{BG}. For a positive gate bias,

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MoS_2 goes into accumulation mode, which is reflected by the increased n_s along with a reduced barrier height with graphene. The opposite result is observed with the negative gate bias. The effective barrier height varied within 0.24-0.91 eV range, which is a range of ~600 meV, showing that current control over 10^{10} may be possible. The presence of low intensity light (10 W/m^2) lowered the barrier by about 0.04 eV for all V_{BG}, and increase in n was also observed (Figure 4.8).

Figure 4.10 shows the variation in barrier height as a function of V_{BG} from current voltage (I-V) and capacitor-voltage (C-V) measurements. Both measurements indicate a ~0.04 eV drop in barrier height when the device was illuminated by a white light source with peak optical power of 10 W/m^2 at ~800 nm wavelength. The corresponding change in carrier concentration (n), obtained from C-V measurements, is shown in Figure 4.11.

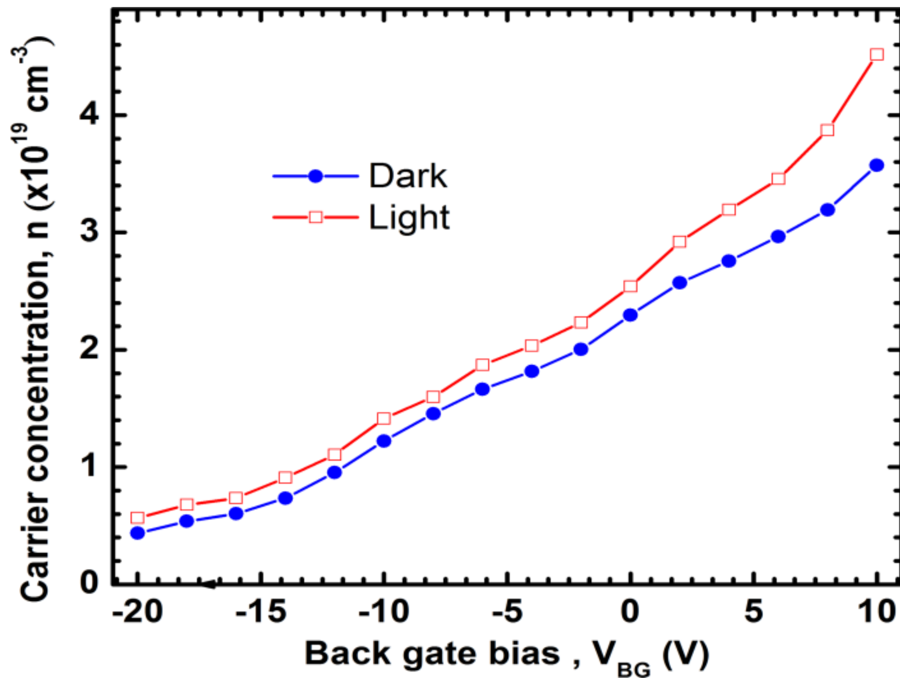

Figure 4.11: Carrier concentration (n) variation obtained from the C-V measurements in Figure 4.10.

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4.3 Band Diagram of the Barristor Device

Based on the above results, the band diagrams and charge balance of the barristor device are shown in Figure 4.12 for (a) V_{BG} >> 0 V (b) V_{BG} << 0 V. The key difference between this structure and traditional Schottky structures is that the constituent materials of this junction are 2D materials, and are thus, very thin. This leads to incomplete screening of the back-gate induced electric field in the bottom MoS_2 layer from the top graphene layer, leading to electric-field modulation in both components of the Schottky junction. Such functionality, enabled by incomplete field screening, is unique to ultra-thin material systems, most practically realized with 2D materials.[13] Since the gate oxide is very thick, and does not leak,[21] charge neutrality must hold in the structure. From a charge-balance electrostatic analysis in the extreme cases, i.e. V_{BG} >> 0 V, and V_{BG} << 0 V, treating the degenerately doped Si substrate as a metal, the origin of Schottky barrier modulation can be understood. At these extreme points, much beyond the flat band voltage in either direction,[21] the influence of interfacial fixed charge is minimal, simplifying the analysis i.e. the charge in the silicon back gate completely overwhelms any sheet fixed interfacial charge in the dielectric (Figure 4.12).

For V_{BG} >> 0 V, large positive mobile sheet charge in the metallic silicon, Q_M, is induced. This must be balanced by negative net mirror charge in the MoS_2, $Q_{MoS2,}$ and graphene, Q_G i.e. $Q_{MoS2} + Q_M < 0$. For V_{BG} >> 0 V, mobile electrons are induced in the MoS_2 (as seen in the transfer curves in Figure 4.4). Furthermore, since the applied field is incompletely screened in MoS_2, the rest of the negative balance charge must be accommodated in the graphene. The $Q_G < 0$ is achieved by a Fermi level above the graphene Dirac K-point in the band-diagram, similar to that seen by [14]. At V_{BG} = +10 V,

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the electron concentration in MoS_2 from C-V (Figure 4.11) is ~4×10^{19} cm^{-3}, corresponding to a Debye screening length[29] of ~0.4 nm. This means that the thickness of the MoS_2 is ~3-5 × the Debye length, leading to ~90-99% screening of the electric field from the back-gate. Thus, only a small portion of the field must be accommodated in the graphene, which is why Q_G is small in this case (Figure 4.12a).

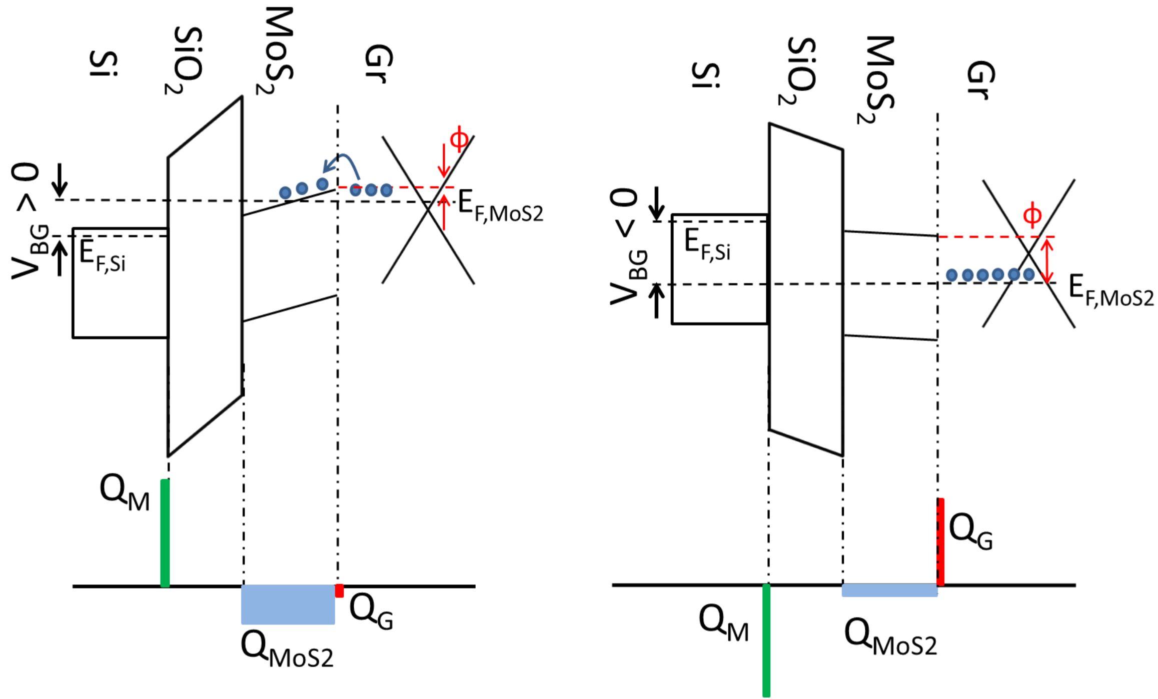

Figure 4.12: Band diagram of the barristor device in thermal equilibrium (V_{DS} = 0 V), showing the Schottky barrier height (φ) for (a) positive and (b) negative gate biases. The charge balance diagrams are shown below each band diagram.

Conversely, for $V_{BG} << 0$ V, $Q_M < 0$ is induced, which must be balanced by Q_{MoS2} and $Q_G > 0$. Since for $V_{BG} << 0$ V, the electron concentration in MoS_2 is reduced to n = 0.4×10^{19} cm^{-3} at V_{BG} = -20 V (Figure 4.11), corresponding to a Debye length of ~1.2 nm which is comparable to the MoS_2 thickness. It means that only ~30-50% of V_{BG} is screened from the graphene. Thus, a significant portion of the mirror charge to negative Q_M must be accommodated in the graphene, leading to $Q_G >> 0$, which is achieved by a fermi level below the graphene Dirac K-point (Figure 4.12b).

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We note that the graphene K-point i.e. graphene conduction band edge, does not need to shift with respect to the conduction band edge of MoS_2, consistent with the general assumption in band line-up theory[30] and other reports of graphene barristors.[14] Finally, the large modulation of Φ from 0.24-0.91eV in this study shows the effective transmission of the electric field from the back-gate to the Schottky junction, showing that the influence of trapped charges in the dielectric is small. Larger modulation of Φ may be achieved by increasing the capacitive coupling of the gate to the Schottky junction i.e. reducing oxide thickness, and/or using high-k dielectrics, without compromising the quality of the dielectric/semiconductor interfaces. This would enable more of the applied V_{BG} to be transmitted to the Schottky junction, leading to greater modulation of Φ or a reduction in the range of V_{BG} to achieve the same modulation of Φ.

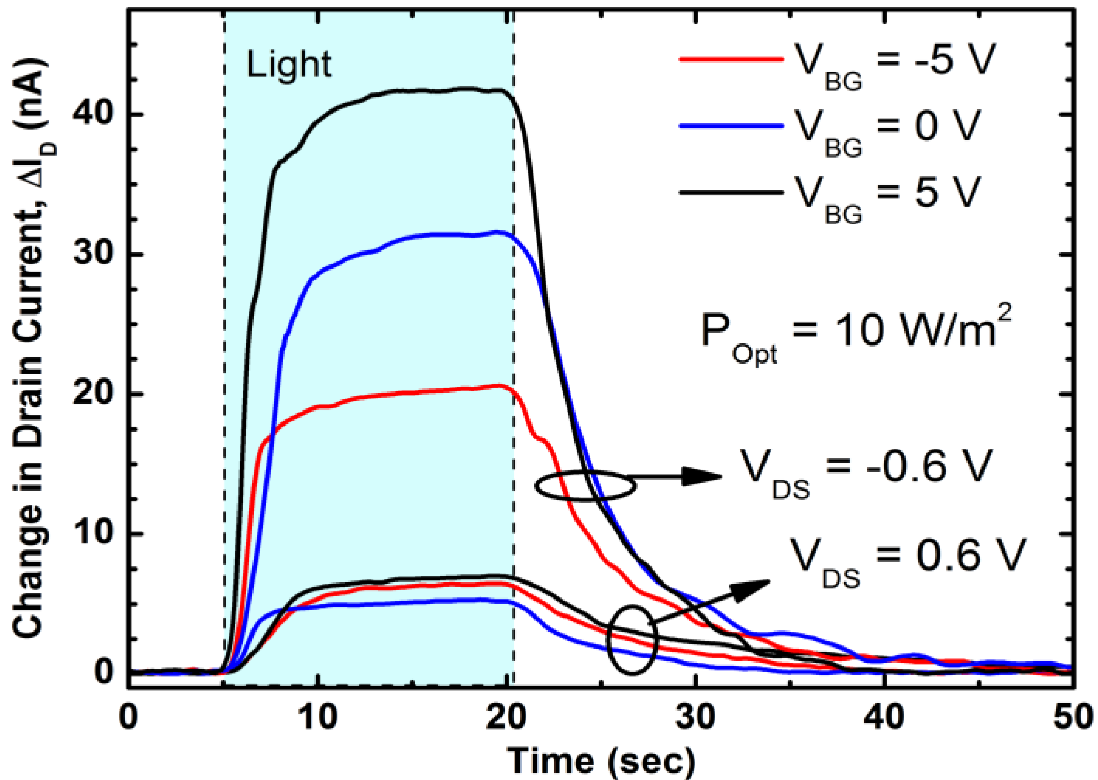

Figure 4.13: Photo response of the barristor device at different gate and drain bias voltages.

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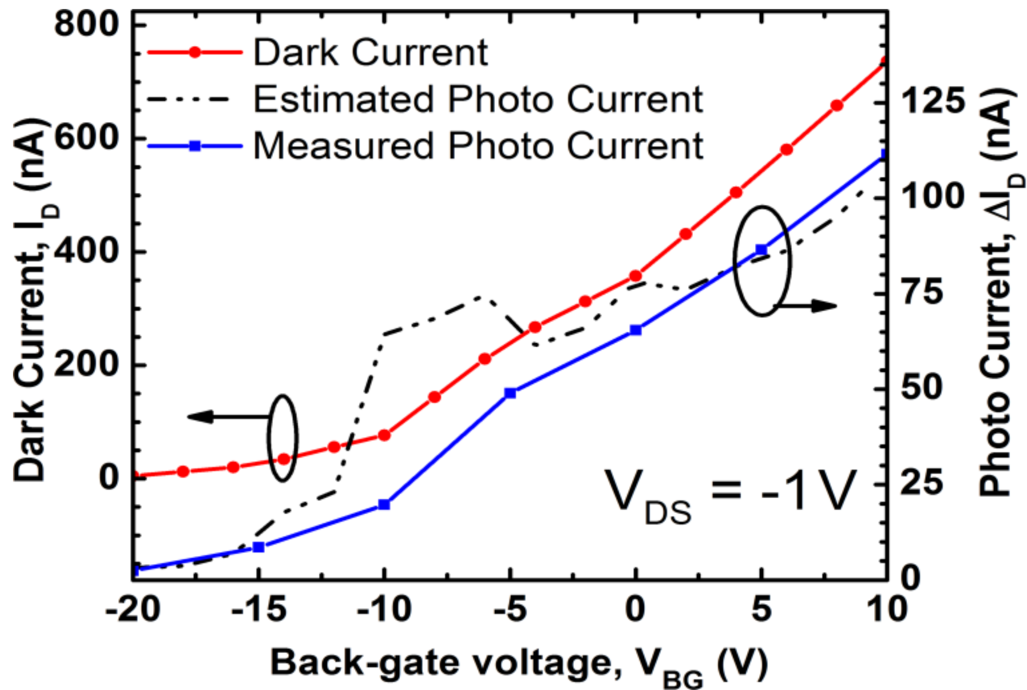

Figure 4.14: Transfer curve of the barristor at V_{DS} = -1 V in the dark, which is used to calculate the estimated photo response by taking the photo-induced barrier height lowering. The measured photo response closely matches with it.

4.4 Optical Response

Figure 4.13 shows the response of the device to light with 10 W/m^2 or 1 mW/cm^2 of optical power from a halogen lamp with color temperature 3350 K, and a peak wavelength of ~800 nm, close to the MoS_2 bandgap of ~850nm (1.45 eV).[13] Electron-hole pairs are generated in the MoS_2 by above bandgap light, which are collected by the electric field at the Schottky junction. Three different V_{BG} steps (-5, 0 and 5 V) were used, while the source-drain Schottky junction, V_{DS} was either forward biased or reverse biased at 0.6 V. The photocurrent was smaller for V_{DS} = +0.6 V as the electric field at the forward-biased Schottky junction was reduced, reducing charge collection, while the converse was true for V_{DS} = -0.6 V. From the C-V measurements, the built-in voltage under illumination decreased by ~0.04 V (from 1/C^2 intercept, Figure 4.8 and Figure

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4.10), across all ranges of V_{BG}, indicating that the reverse leakage current of the diode increases under illumination. In this V_{BG} range, the electron density is high enough for the conduction band and the Fermi level to be considered identical,[29] indicating that the Schottky barrier changes by ~0.04 eV as well. For example, Φ is large for V_{BG} = -5 V and V_{DS} = -0.1 V, leading to lower the overall leakage current levels, while the reverse is true for V_{BG} = +5 V. Using the transfer curve from I-V in Figure 4.9, and the change in Φ estimated from the C-V curves in Figure 4.10, the expected change in I_{DS} can be predicted (Figure 4.14), and is consistent with the photocurrents actually measured in Figure 4.13.

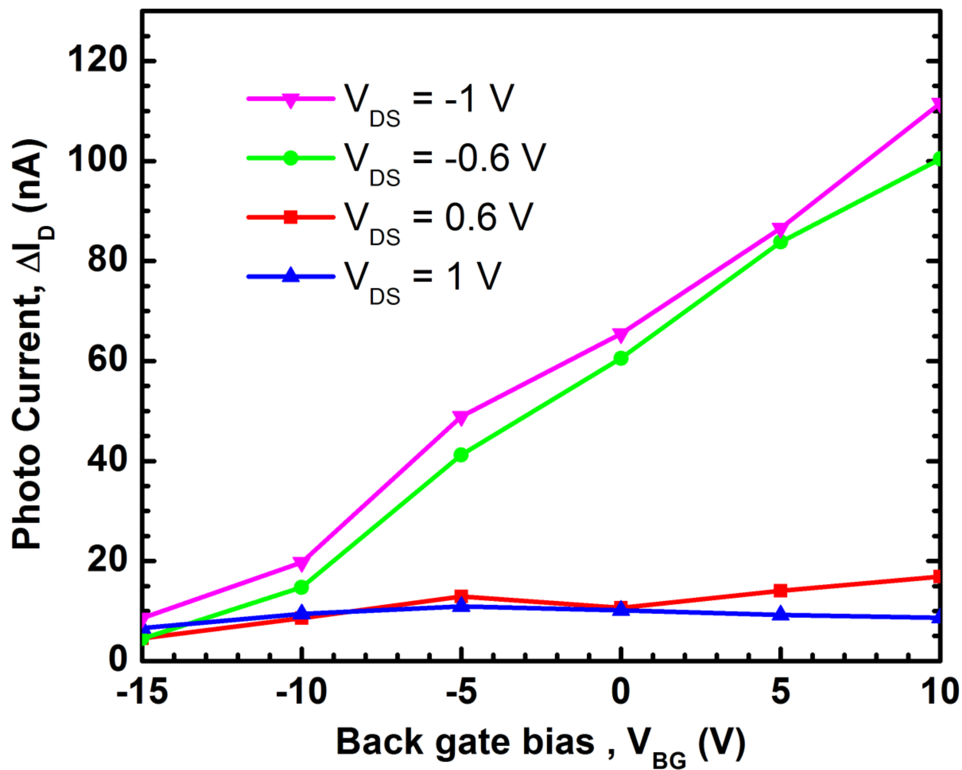

Figure 4.15: Photocurrent at 10 W/m^2 optical power, measured for different grate and drain biases.

In Figure 4.14, we show the dark current and the photo current for V_{DS} = -1 V along with the expected photocurrent based on the change in barrier height in presence of

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light. For this calculation, we resorted to the Φ(C-V) vs. V_{BG} curves in Figure 4.10 with and without light. For each point on the Φ(light) curve, the same value was located on the Φ(dark) curve and the corresponding V_{BG} was calculated through interpolation. Using that effective V_{BG}, the total current under illumination was estimated from the dark transfer characteristics (Figure 4.9). After subtracting the dark current, we obtained the photocurrent which matched very closely with the experimental photocurrent (Figure 4.14). Thus, the photocurrent difference due to the variation in V_{DS} can be attributed to the changes in charge collection, whereas that due to the changes in V_{BG} is due to the variations in reverse leakage in the thermionic emission phenomenon ((4) - (6)), which give opposing photo-response trends.

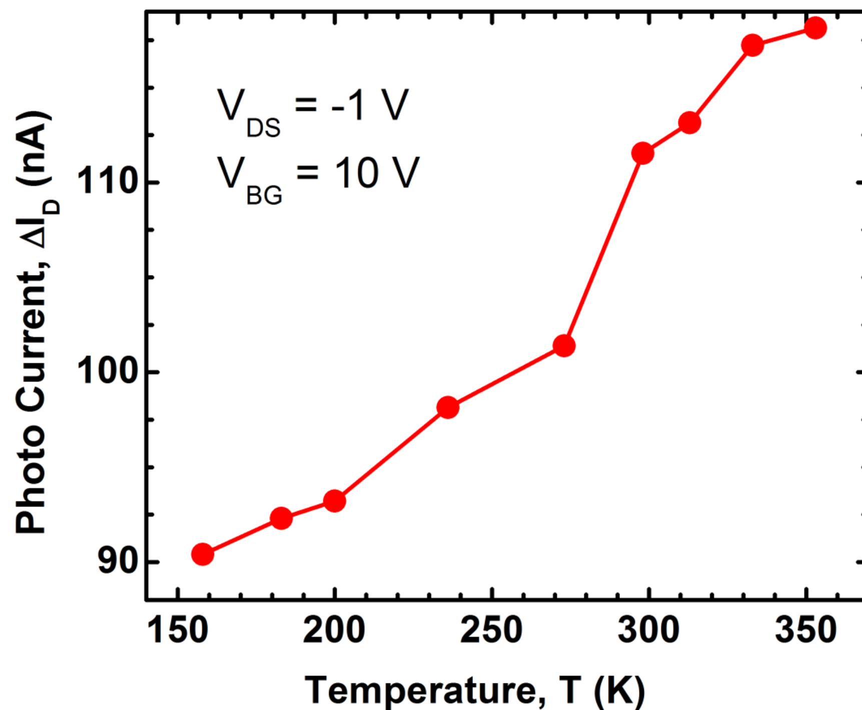

Figure 4.16: Effect of temperature on the photocurrent at fixed bias conditions.

The responsivity was estimated by accounting for the device area i.e. by using the optical power incident on the 5 × 100 μm^2 device, and the total measured photocurrent.

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This gave a peak responsivity of ~20 A/W at V_{BG} = 10V and V_{DS} = -0.6 V. Even 100% external quantum efficiency would correspond to a responsivity of ~0.2 A/W, which indicates that there is gain in this device. Moreover, due to the very thin layers, only a fraction of the incident light will be absorbed, providing further evidence of internal gain. Given the slow response time of this device, ~10s, the high optical optical responsivity is likely due to photoconductive gain in the Schottky junction,[32] as an RC limited response time of <1 ms would have been expected (Figure 4.6 and Figure 4.8). Photoconductive gain is also supported by C-V (Figure 4.8 and Figure 4.11), where the majority carrier concentration increases under illumination.

In Figure 4.15, we show the variation in photocurrent (ΔI_D) for V_{BG} = -15 to 10 V and V_{DS} = ± 0.6 V and ±1 V. Here, ΔI_D increased further with a more negative V_{DS} (-1 V), and the maximum of about 110 nA was recorded at room temperature for the reverse bias mode. The minimum ΔI_D occurred at -15 V of V_{BG}, due to the large barrier and increased MoS_2 series resistance. Although ΔI_D did not seem to saturate at its maximum value of ~ 110 nA, it could not increase indefinitely with a more negative V_{DS} or a more positive V_{BG}.

A large reverse bias voltage would increase the current to a level where series resistance would start to dominate and thus limit ΔI_D. Similarly a more positive V_{BG} would lower the barrier height to an extent where the current would increase significantly and experience the same problem with series resistance. On the other hand, ΔI_D is much smaller in the forward bias (V_{DS} = 0.6 V and 1 V) region with an interesting trend. At V_{DS} = 0.6 V, ΔI_D slowly increases as V_{BG} becomes more positive, which is consistent with the trend observed in reverse bias. But at V_{DS} = 1 V, ΔI_D first increases and then

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decreases with V_{BG}. This happens because of the increased dark current level at V_{DS} = 1 V which makes the series resistance to become prominent as V_{BG} increases and thus lower the photocurrent. Figure 4.16 shows the effect of temperature (T) on the ΔI_D in the reverse bias condition (V_{BG} = 10 V, V_{DS} = -1 V). Since the junction current increases with T, so does the ΔI_D. However, ΔI_D tends to saturate at temperatures above 330 K due to the device resistance going up quickly.

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Chapter 5

Graphene/MoS_2 Barristor: Sensing Experiments and Results

In this chapter, we continue our discussion on graphene/MoS_2 barristor from the last chapter and focus on the sensing applications of this novel device. While graphene is inherently sensitive to many chemical species, the sensitivity can be further enhanced by operating a graphene-based device in the exponential (i.e. subthreshold) regime of the transfer curve. This can be achieved conveniently by a barristor device, where a gate bias can be used to tune the barrier height and hence the transport mechanism. Since we have demonstrated the greatest barrier height modulation for any graphene-based barristor in the previous chapter, it is expected that a high degree of tunability can also be achieved in the sentivity of the graphene/MoS_2 barristor device.

5.1 Types of Sensors

A chemical sensor is a device that transforms chemical information, ranging from the concentration of a specific sample component to total composition analysis, into an analytically useful signal. The chemical information, mentioned above, may originate from a chemical reaction of the analyte or from a physical property of the system.

A physical sensor is a device that provides information about a physical property of the system. A chemical sensor is an essential component of an ***analyzer.*** In addition to the sensor, the analyzer may contain devices that perform the following functions: sampling, sample transport, signal processing, data processing. An analyzer may be an

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essential part of an automated system. The analyzer working according to a sampling plan as a function of time acts as a monitor.

Chemical sensors contain two basic functional units: a receptor part and a transducer part. Some sensors may include a separator which is, for example, a membrane. In the ***receptor*** part of a sensor the chemical information is transformed into a form of energy which may be measured by the transducer.

The ***transducer*** part is a device capable of transforming the energy carrying the chemical information about the sample into a useful analytical signal. The transducer as such does not show selectivity.

The receptor part of chemical sensors may be based upon various principles:

- Physical, where no chemical reaction takes place. Typical examples are those based upon measurement of absorbance, refractive index, conductivity, temperature or mass change.

- Chemical, in which a chemical reaction with participation of the analyte gives rise to the analytical signal.

- Biochemical, in which a biochemical process is the source of the analytical signal. Typical examples are microbial potentiometric sensors or immunosensors. They may be regarded as a subgroup of the chemical ones. Such sensors are called ***biosensors.***

In some cases it is not possible to decide unequivocally whether a sensor operates on a chemical or on a physical principle. This is, for example, the case when the signal is due to an adsorption process.

Sensors are normally designed to operate under well-defined conditions for

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specified analytes in certain sample types. Therefore, it is not always necessary that a sensor responds specifically to a certain analyte. Under carefully controlled operating conditions, the analyte signal may be independent of other sample components, thus allowing the determination of the analyte without any major preliminary treatment of the sample. Otherwise unspecific but satisfactory reproducible sensors can be used in series for multicomponent analysis using multivariate calibration software and signal processing. Such systems for multicomponent analysis are called sensor arrays.

The development of instrumentation, microelectronics and computers makes it possible to design sensors utilizing most of the known chemical, physical and biological principles that have been used in chemistry.

Chemical sensors may be classified according to the operating principle of the transducer:

1. ***Optical devices*** transform changes of optical phenomena, which are the result of an interaction of the analyte with the receptor part. This group may be further subdivided according to the type of optical properties which have been applied in chemical sensors:

a) Absorbance, measured in a transparent medium, caused by the absorptivity of the analyte itself or by a reaction with some suitable indicator.

b) Reflectance is measured in non-transparent media, usually using an immobilized indicator.

c) Luminescence, based on the measurement of the intensity of light emitted by a chemical reaction in the receptor system.

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d) Fluorescence, measured as the positive emission effect caused by irradiation. Also, selective quenching of fluorescence may be the basis of such devices.

e) Refractive index, measured as the result of a change in solution composition. This may include also a surface plasmon resonance effect.

f) Optothermal effect, based on a measurement of the thermal effect caused by light absorption.

g) Light scattering, based on effects caused by particles of definite size present in the sample.

2. ***Electrochemical devices*** transform the effect of the electrochemical interaction analyte – electrode into a useful signal. Such effects may be stimulated electrically or may result in a spontaneous interaction at the zero-current condition. The following subgroups may be distinguished:

a) Voltammetric sensors, including amperometric devices, in which current is measured in the d.c. or a.c. mode. This subgroup may include sensors based on chemically inert electrodes, chemically active electrodes and modified electrodes. In this group are included sensors with and without (galvanic sensors) external current source.

b) Potentiometric sensors, in which the potential of the indicator electrode (ion-selective electrode, redox electrode, metal-metal oxide electrode) is measured against a reference electrode.

c) Chemically sensitized field effect transistor (CHEMFET) in which the effect of the interaction between the analyte and the active coating is transformed into a change of the source-drain current. The interactions between the analyte and the coating are, from the

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chemical point of view, similar to those found in potentiometric ion-selective sensors.

d) Potentiometric solid electrolyte gas sensors, differing from class 2(b) because they work in high temperature solid electrolytes and are usually applied for gas sensing measurements.

3. ***Electrical devices*** based on measurements, where no electrochemical processes take place, but the signal arises from the change of electrical properties caused by the interaction of the analyte.

a) Metal oxide semiconductor sensors used principally as gas phase detectors, based on reversible redox processes of analyte gas components.

b) Organic semiconductor sensors, based on the formation of charge transfer complexes, which modify the charge carrier density.

c) Electrolytic conductivity sensors.

d) Electric permittivity sensors.

4. ***Mass sensitive devices*** transform the mass change at a specially modified surface into a change of a property of the support material. The mass change is caused by accumulation of the analyte.

a) Piezoelectric devices used mainly in gaseous phase, but also in solutions, are based on the measurement the frequency change of the quartz oscillator plate caused by adsorption of a mass of the analyte at the oscillator.

b) Surface acoustic wave devices depend on the modification of the propagation velocity of a generated acoustical wave affected by the deposition of a definite mass of the analyte.

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5. ***Magnetic devices*** based on the change of paramagnetic properties of a gas being analysed. These are represented by certain types of oxygen monitors.

6. ***Thermometric devices*** based on the measurement of the heat effects of a specific chemical reaction or adsorption which involve the analyte. In this group the heat effects may be measured in various ways, for example in the so called catalytic sensors the heat of a combustion reaction or an enzymatic reaction is measured by use of a thermistor. The devices based on measuring optothermal effects can alternatively be included in this group.

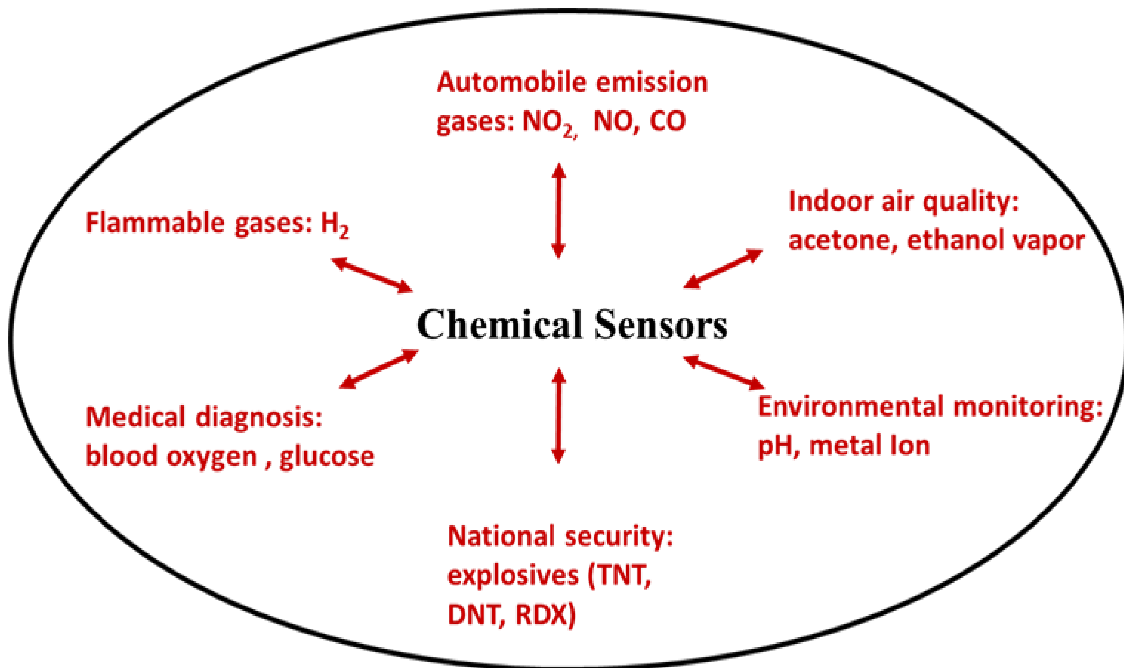

Figure 5.1 Various applications of chemical sensors

Figure 5.1 shows various applications of chemical sensors including monitoring automobile emission gasses, medical diagnosis, industrial control, national security, indoor air quality control, and environmental evaluation.

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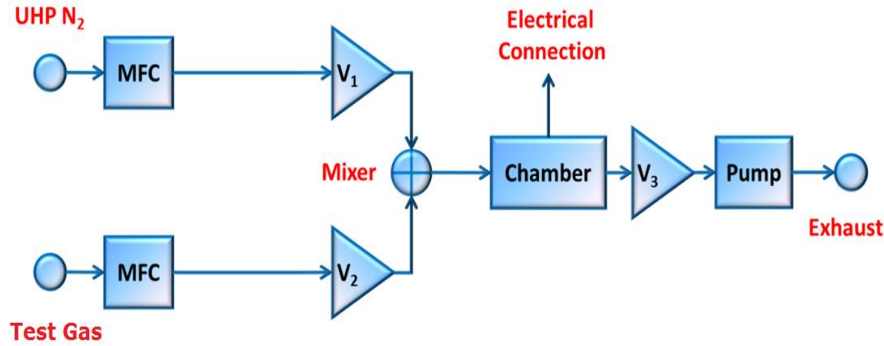

Figure 5.2: VOC sensing setup.

5.2 Sensing Setup

Sensing experiments were done in a small chamber, which housed the wire-bonded sample. The chamber had an inlet and an outlet; wires from the device were taken out through a small opening near the outlet, which was stuffed with Teflon tape. A roughing pump along with a valve (V_3 in Figure 5.2) was connected to the outlet to quickly remove the analyte vapor out of the chamber whenever necessary. The inlet side of the chamber had a mixer assembly – consisting of a mixer junction with valves, two mass flow controllers. One mass flow controller was used to flow ultra-high purity (UHP) N_2, the other one was used to flow the test gas. Both N_2 and the test gas lines had two valves (V_1 and V_2, respectively) connected to them to control the flow of the gas and eventually merged into the mixer junction, which directed the gas mixture into the inlet of the chamber. The purpose of using the mixer was to dilute test gas with UHP N_2 to obtain different concentrations, hence the flow rate of both MFCs were adjusted to get the desired ratio of N_2 and test gas. After each sensing experiment, V_2 (vapor flow valve) was closed, but V_1 and V_3 were kept open. As a result, UHP N_2 flushed the chamber while the pump connected to V_3 quickly took out the residual gas mixture from the chamber.

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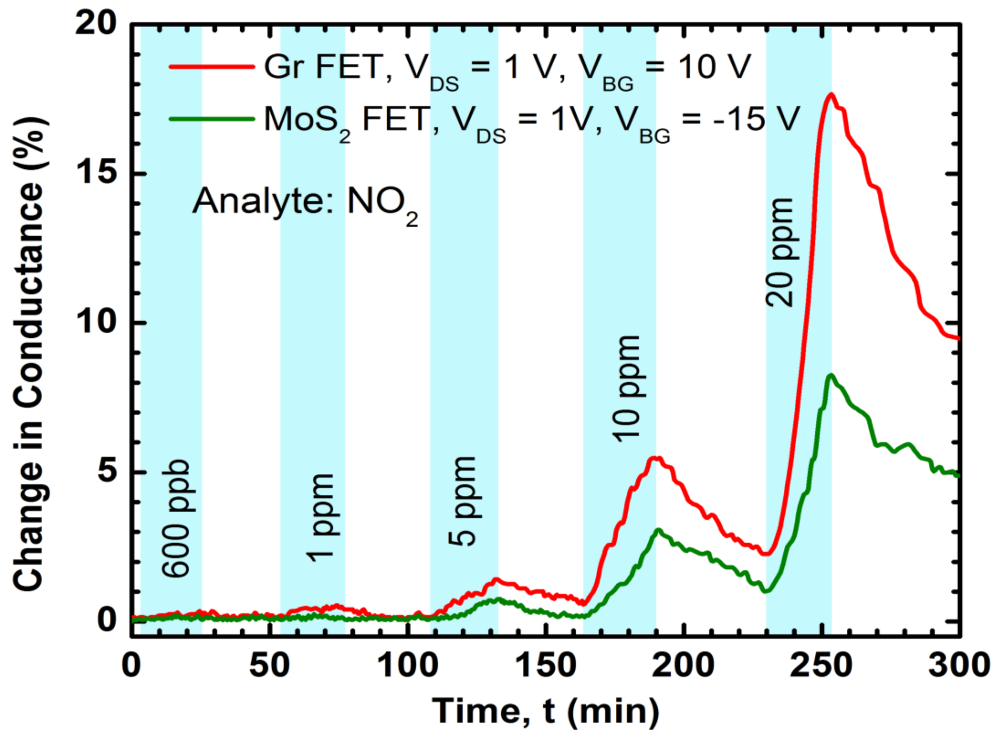

Figure 5.3: Percentage changes in conductance of Graphene and MoS_2 based FETs on 100 nm SiO_2/Si to various concentrations of NO_2.

The response of the device to the test gas was evaluated in two ways – (1) change in current (conductance) at constant bias condition, and (2) change in junction capacitance at constant bias conditions. For current-based measurements, an Agilent B2902 source measuring unit (SMU) was used, while for capacitance-based measurements a HP4284A precision LCR meter was used. The test gases used in this work are NO_2 and NH_3, which are commonly used to benchmark the performance of various graphene-based gas sensors. All experiments were performed at room temperature and in dark environment, to avoid any interference that may arise from the strong photoresponse of the device.

5.3 Conductance-based Sensing Experiments

Since CVD graphene is p-type and NO_2 serves as an acceptor for graphene,[1][2] it

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increases the conductivity in graphene. In Figure 5.3, the changes in conductance are shown for both MoS_2 and graphene based FETs for appropriate bias conditions. For GFET (i.e. Graphene FET), V_{BG} = 10 V is just around the Dirac point (Figure 4.4); while for the MFET (i.e MoS_2 FET), V_{BG} = -15 V is deep inside the depletion/inversion regime, where a significant hole current is also present due to the weak inversion of MoS_2. For both cases, NO_2 acts as an acceptor; although charge transfer is weaker in the MFET, as seen from the smaller change in conductnce. In Figure 5.4, we see the response of the graphene/MoS_2 heterojunction device to 800 ppb of NO_2, at different gate voltages and V_{DS} = -1 V in dark environment.

Interestingly, here the barristor current increases as well, which means the barrier height is reducing in presence of NO_2. In the heterojunction, graphene is on top and will adsorb the gas molecules, so any change in barrier height can be attributed to the change in graphene Fermi level. However, presence of an acceptor should move the graphene Fermi level in downwards direction, and thus increase the barrier height. Instead, a reduced barrier height is apparent due to the increased conductance, which means the graphene Fermi level is moved to the point where NO_2 acts as a donor. Another possibility is the combined effect of graphene and MoS_2 being exposed to NO_2, due to the partial screening of any electric field in graphene, which may also result in the NO_2 acting as a donor.Since the change in current is highly nonlinear at reverse bias and the current decreases further at negative gate bias (Figure 4.6), the percentage change in conductance is observed to be more pronounced (Figure 5.4) at negative V_{BG} due to the smaller base current, negligible series resistance and higher slope of the transfer characteristics in log scale.

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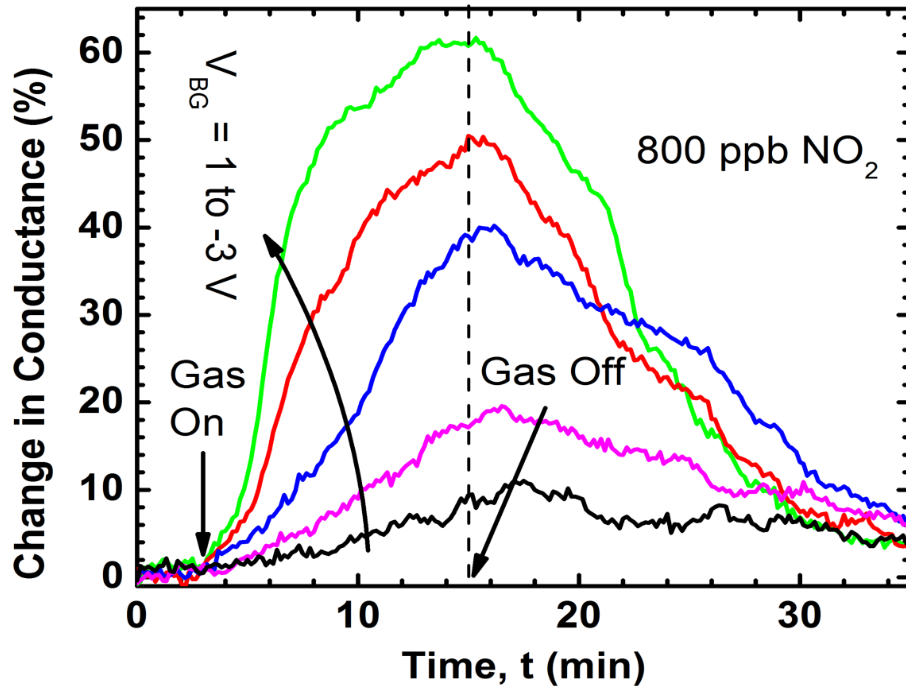

Figure 5.4: Percentage change in conductance of Graphene/MoS_2 heterojunction FET on 100 nm SiO_2/Si to 800 ppb of NO_2 at various gate biases and for V_{DS} = -1 V (dark).

Figure 5.5 shows the response of the barristor device to various concentrations of NO_2 at V_{BG} = -3 V, V_{DS} = -1 V (dark). For 20 ppm concetration, the response magnitude of the barristor device is about 20 times greater than the GFET and about 50 times greater than the MFET, which highlights the improved sensitivity that can be achieved using this device. This high sensitivity is attributed to the barrier height change in the vertical heterojunction, which causes a sharper change in conductance than the planar GFET and the MFET devices. While MFET is also in exponential regime (subthreshold regime, in weak inversion), the charge transfer to MoS_2 in generally weaker due to the difficulty in the adsoprtion process.[3] As a result, by properly tuning the backgate bias, the lowest concentration level that could be detected was ~100 ppb, which was far better than a simple GFET.

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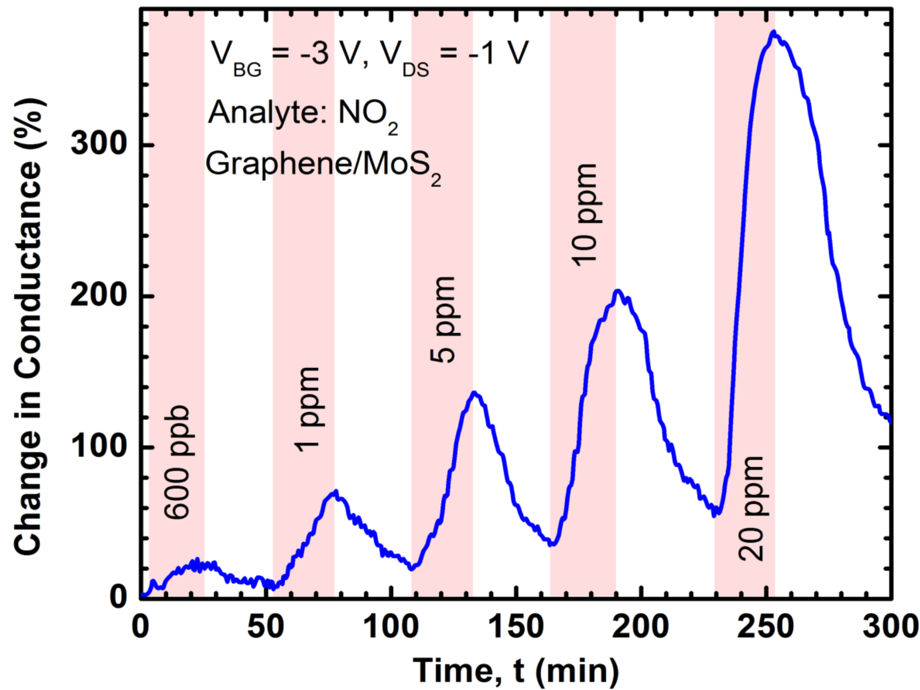

Figure 5.5: Percentage change in conductance of Graphene/MoS_2 heterojunction FET on 100 nm SiO_2/Si to various concentrations of NO_2 at V_{BG} = -3 V, V_{DS} = -1 V (dark).

In Figure 5.6, we see the responses of the GFET, MFET and the barristor device to different concentrations of NH_3 at the same bias conditions as shown in Figure 5.3 and Figure 5.5. NH3 is a donor for graphene at near Dirac point and MoS_2 at weak inversion, which means the carrier concentration is reduced and so does the conductance. However, in the barristor configuration, NH_3 behaves like an acceptor as it increases the barrier height to reduce reverse bias current. It means the effective work function of NH_3 adsorped to the graphene/MoS_2 composite changes to the point that it becomes an acceptor. Besides, the charge transfer also increases significantly as seen in Figure 5.6, where at 550 ppm concentration, the barristor response is 7-10 times greater than the GFET and the MFET devices. The lowest concentration that could be detected using the barristor was about 1 ppm, by tuning the gate and drain bias voltages.

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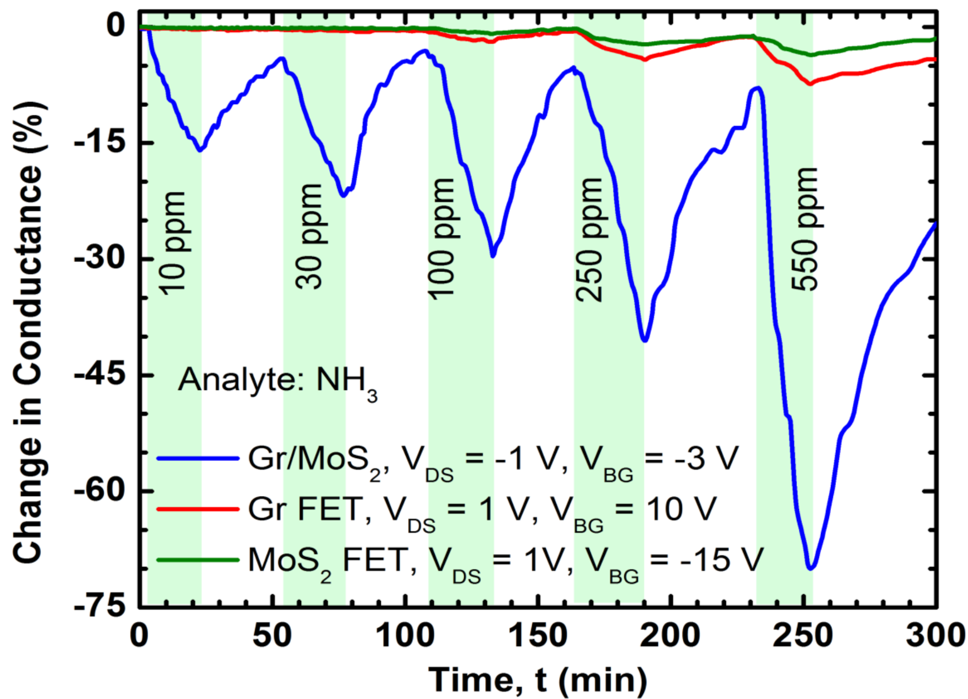

Figure 5.6: Percentage change in conductance of graphene FET, MoS_2 FET and Graphene/MoS_2 heterojunction FET on 100 nm SiO_2/Si to various concentrations of NH_3.

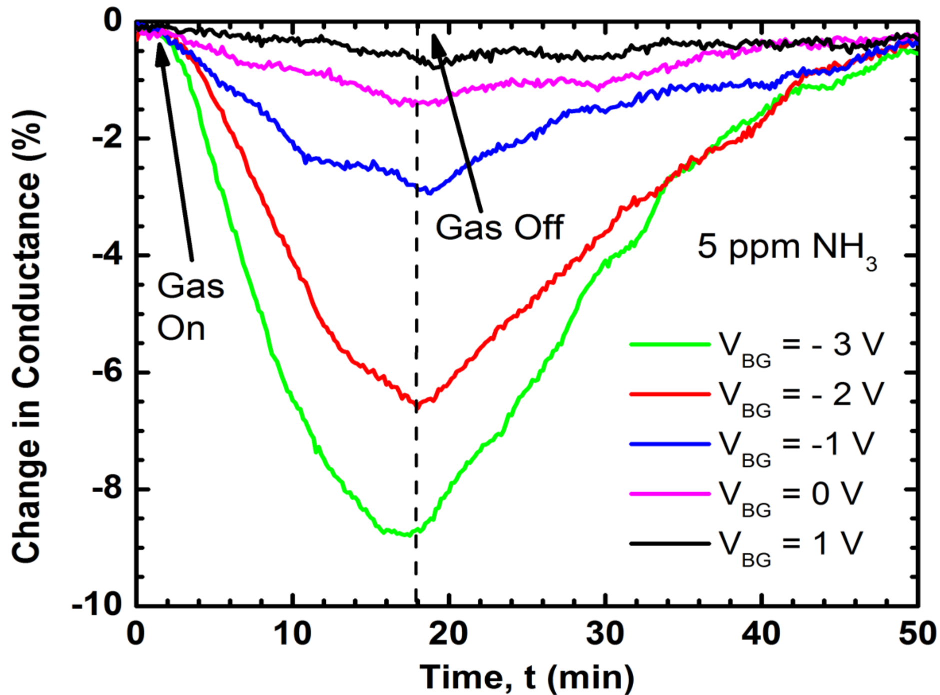

Figure 5.7: Percentage change in conductance of Graphene/MoS_2 heterojunction FET on 100 nm SiO_2/Si to 5 ppm of NH_3 at various gate biases and for V_{DS} = -1 V.

In Figure 5.7, we see how the bias voltage affects the response of the barristor.

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Just like NO_2, the best sensitivity to NH_3 also came at reverse gate bias voltages as shown in this figure.

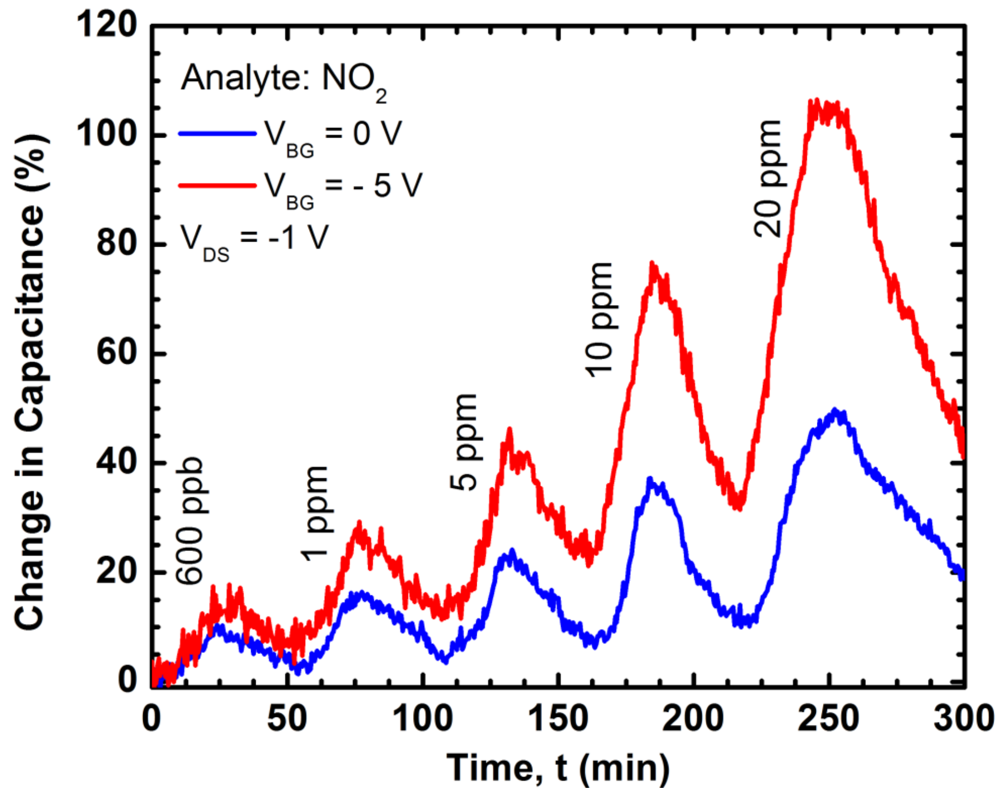

Figure 5.8: Percentage change in junction capacitance of Graphene/MoS_2 heterojunction FET on 100 nm SiO_2/Si to various concentrations of NO_2 at V_{BG} = 0 and -5 V, V_{DS} = -1 V (dark).

5.4 Capacitance-based Sensing Experiments

The C-V measurement in presence of an analyte provides direct insight into the barrier height related information of the heterojunction. Measuring capacitance at fixed bias conditions (V_{BG}, V_{DS}) as a function of time in presence of various concentrations of an analyte shows how quickly these changes take place, as is shown in Figure 5.8. Here, we see that the rise/fall times are in the order of 10s of minutes, which is not surprising for large area graphene based chemical sensors at low analyte concentrations. Since graphene has very low sticking coefficient, most of the molecules hitting the surface of

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graphene does not readily adhere to the surface. That is why a significantly faster response can be expected at much higher concentrations.

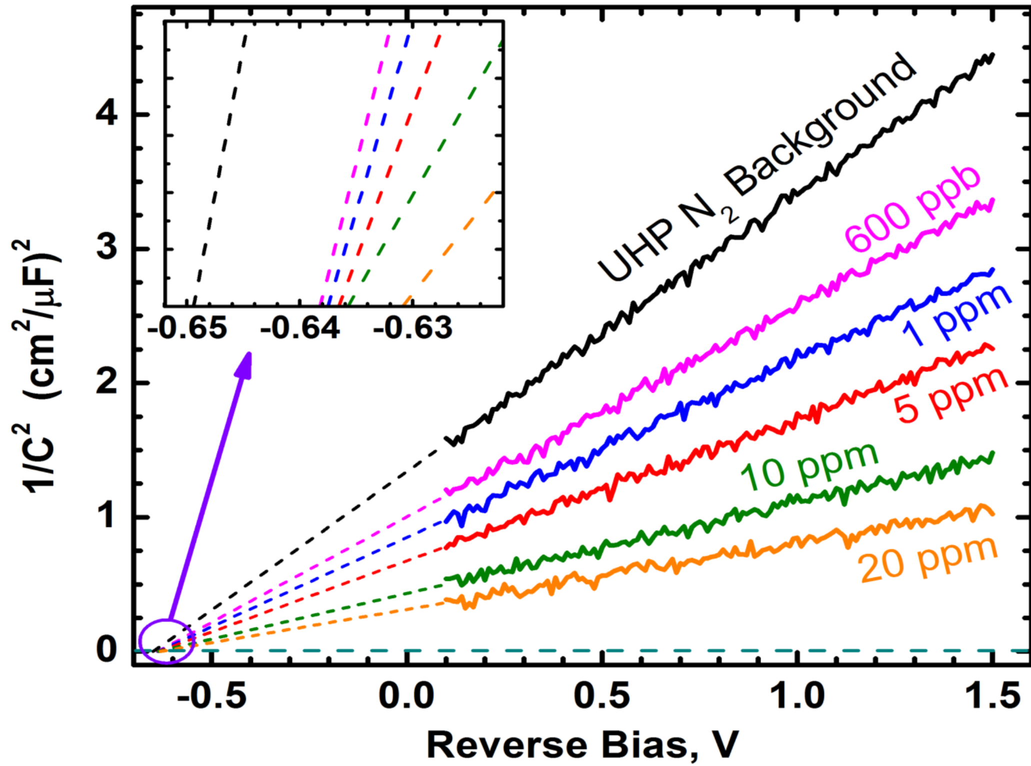

Figure 5.9: $1/C^2$ vs reverse bias for MoS_2/graphene barristor at room temperature for V_{BG} = -5 V, in UHP N_2 ambient and in presence of various concentrations of NO_2. The dashed lines are least square linear fits. The inset shows X-axis intercepts to show the change in barrier heights.

From Figure 5.8, it is clear that the capacitive response of the barristor to NO_2 is consistent with the conductance-based response as shown in Figure 5.4 and Figure 5.5. Figure 5.9 helps to explain why the analytes behave differently when adsorp at the surface of the graphene/MoS_2 composite as opposed to bare graphene or MoS_2. Here, with the help of $1/C^2$ vs. V (reverse biased V_{DS}) curves, we see that the adsorbed NO_2 molecules not only change the barrier height by affecting the Fermi level of graphene, but also affect the carrier concetraion in MoS_2 as well (using (7)). This indicates that the MoS_2, while being underneath graphene, interacts with the NO_2 molecules due to the

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graphene being atomically thin. As a result, the graphene and MoS_2 are not interacting individually with the adsorbed molecules, rather they are acting as a composite with different electronic properties which may reverse the role of NO_2 and NH_3 as dopants. The changes in barrier heights (Φ) and carrier concentrations (n), extracted from the C-V measurements, are shown in Figure 5.10 for various concentrations of NO_2. The change in barrier height is greater for V_{BG} = -5 V, because of the sharper slope of Φ vs V_{BG} curve (Figure 4.9) around this point. Very similar responses were observed for NH_3 as well, but with opposite polarity and somewhat lower sensitivity.

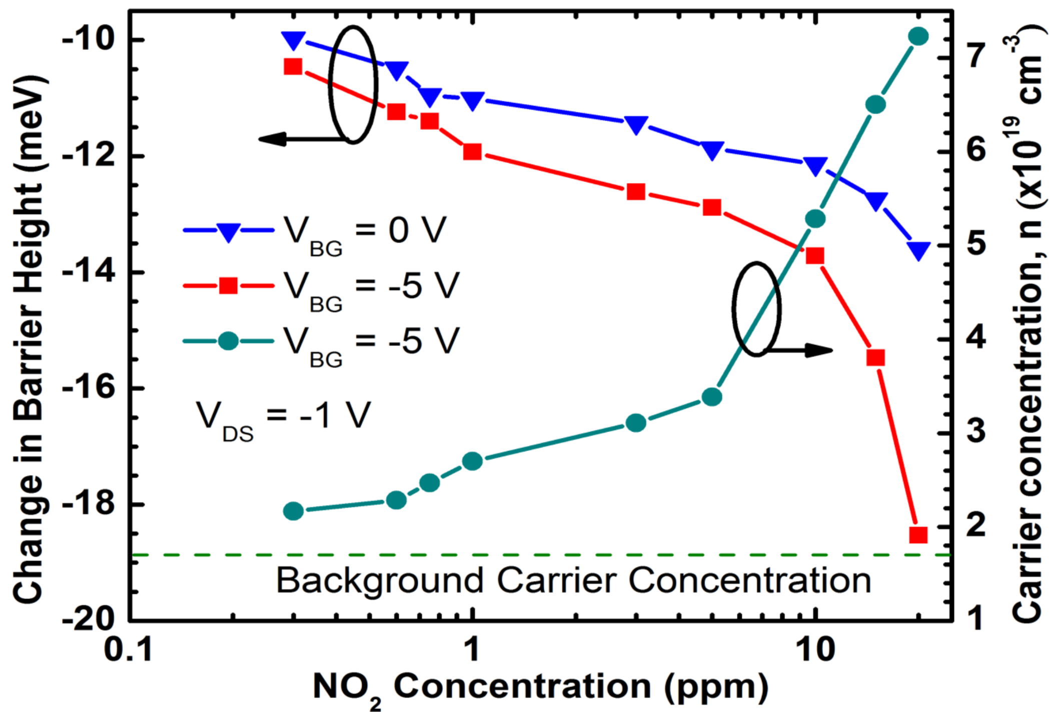

Figure 5.10: Change in barrier height for Graphene/MoS_2 heterojunction FET on 100 nm SiO_2/Si to various concentrations of NO_2 at V_{BG} = 0 and – 5 V, V_{DS} = -1 V (dark), calculated from C-V.

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Chapter 6

Graphene/InN Nanowire Based Mixed Dimensional Barristor

In this chapter, we present a non-conventional barristor device – a heterojunction of graphene and horizontally grown InN nanowires (NW). This is an example of a mixed dimensional heterojunction, combining a 2D material (graphene) with 1D nanowires. Here we start our discussion with a brief description of InN NW synthesis and basic characteristics, followed by the fabrication of graphene/InN NW heterojunction. Since InN has a high surface accumulation of electrons, forming a Schottky barrier with graphene is quite challening. We address this issue by controlled oxidation and passivation of the surface using O_2 plasma in an Reactive Ion Etching (RIE) system before forming the heterojunction. This results in a significant improvement in Schottky behavior, allowing the heterojunction to possess versatile applications – such as gas sensing, photo detection, etc. Applying a backgate bias is observed to unlock even more exciting possibilities, by modulating the Schottky barrier and the carrier concentration in both materials, which will be discussed in details in this chapter. Finally, a gate-controllable novel memristor device based on graphene/In_2O_3-InN core-shell NW with thick interfacial In_2O_3 is demonstrated for the first time.

These works are carried out in former Nanoscale Electronics and Sensors Laboratory (NESL) in Dr. Goutam Koley's supervision, and the contribution of Dr. Alina Wilson is especially acknowledged. A greater detail of the growth, fabrication and characterization of InN NW devices can be found in Dr. Alina Wilson's (Franken)

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dissertation and also in the earlier publications[1]-[3]. The first two sections of this chapter are adopted in abridged and modified form her dissertation, the subsequent sections are novel contributions made in this work.

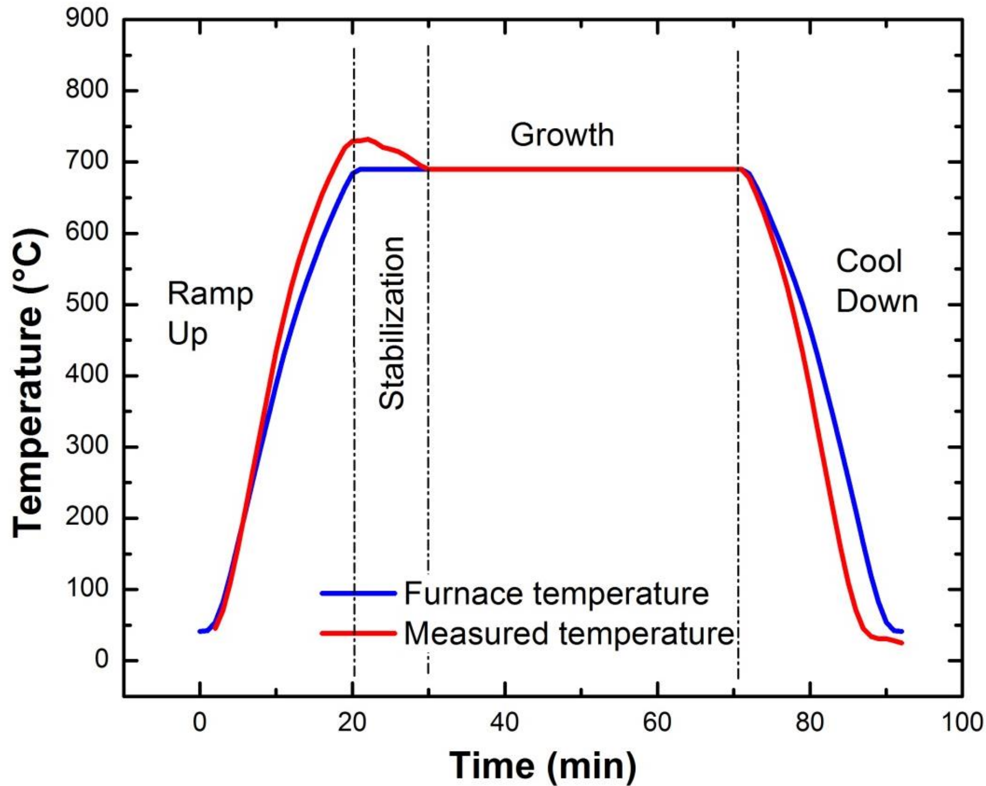

Figure 6.1 Temperature-time curve for InN NW synthesis using a CVD furnace.

6.1 Growth and Characterization of InN Nanowires

One of the most critical parameter for InN growth is the temperature. In order to get high quality InN NWs we need to optimize the temperature and avoid the temperature at which ammonia cracks and the temperature at which the nanowires will decompose. According to previous experiments[nanoscale], a temperature profile is required to control the growth mechanism and the temperature should be kept constantat ~690 ºC, during nanowire growth. There are four modes of temperature control, including ramp-up, temperature stabilization, process flow and cool down, in the temperature profile, as

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shown in Figure 6.1. Once the temperature has ramped up and the furnace temperature controller has reached 690 ºC, a 10 minute wait period is necessary, because during this time the temperature gets stabilized around a constant value. At the beginning of this 10 minute wait period it is observed that the temperature overshoots and reaches 730 ºC which could damage the material quality. After the stabilization time the growth process continues as normal by introducing the required gases into the chamber. Once the growth is done, the furnace is cooled down rapidly by partially opening the furnace and using a fan to blow air towards the closed process tube.

The gases used for the synthesis of InN NWs are UHP NH_3 and dilute O_2 (with N_2 as the carrier gas). O_2 helps in cracking of NH_3 below the usual temperature, using Au patterns as the catalyst beds. Metallic In is also used as another precusros, which forms In vapor that reacts with the N-species released from NH_3.

To verify the structural composition of the, HRTEM imaging of the NWs was performed. Figure 6.2 (a)-(d) show the HRTEM images of the NWs for 2, 4, 10 and 14 sccm of oxygen flow rates respectively, while the insets show the FFT spectra. The lattice resolved TEM images indicate good crystalline quality of the NWs, while the FFT spectra indicate the wurtzite structure for all the oxygen flow rates. To further investigate the chemical composition of these NWs, we performed Energy Dispersive X-ray Spectroscopy (EDX or EDS) analysis on a fixed spot on a thin InN NW and subtracted the contribution of the SiO_2 membrane. The adjusted EDS spectra is shown in Figure 6.3, while the individual spectra obtained on the InN NW and the SiO_2 are shown in the top left inset of Figure 6.3. A TEM image of the NW and the measurement spots are shown in the top right inset of Figure 6.3. To obtain the adjusted spectrum, we subtracted the

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EDS spectrum on the SiO_2 membrane from that obtained on the NW, after multiplying the SiO_2 spectrum with the ratio of the Si peak related photon counts, i.e. the areas under the Si peaks at 1.75 keV. We find that the adjusted spectrum shows no noticeable Si or O peak, which further supports the compositional purity of these NWs.

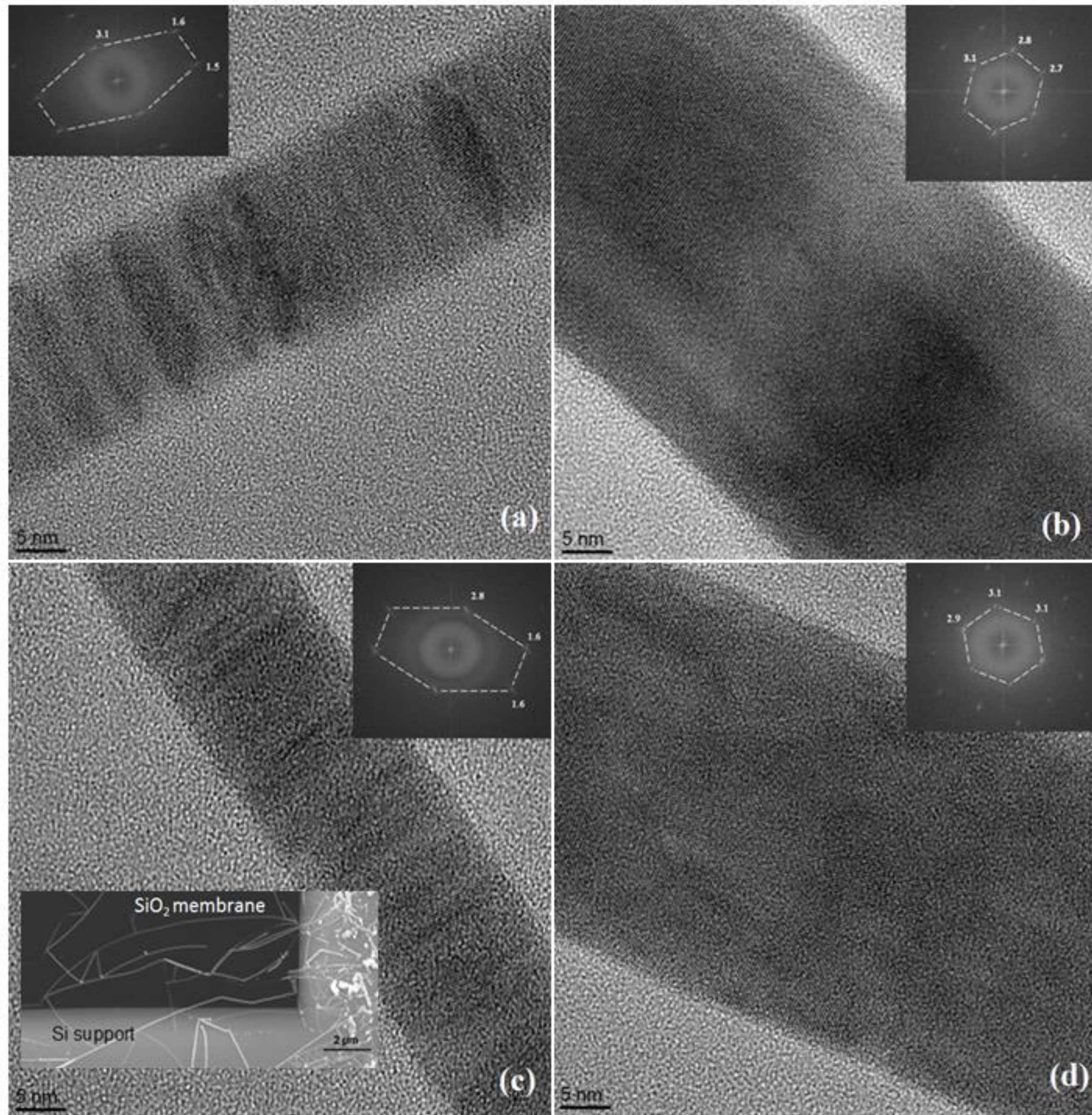

Figure 6.2 HTREM images of single NWs (on 40 nm SiO_2 membranes) grown at different oxygen (3% in balance N_2) flow rates: (a) 2 sccm; (b) 4.0 sccm; (c) 10.0 sccm; (d) 14.0 sccm. Careful observation shows lattice planes in the images. Insets in the images show the respective hexagonal FFT spectra. Bottom left inset of (c) shows a typical SiO_2 membrane window with NWs growing from catalyst spots on the Si support to the SiO_2 membrane.

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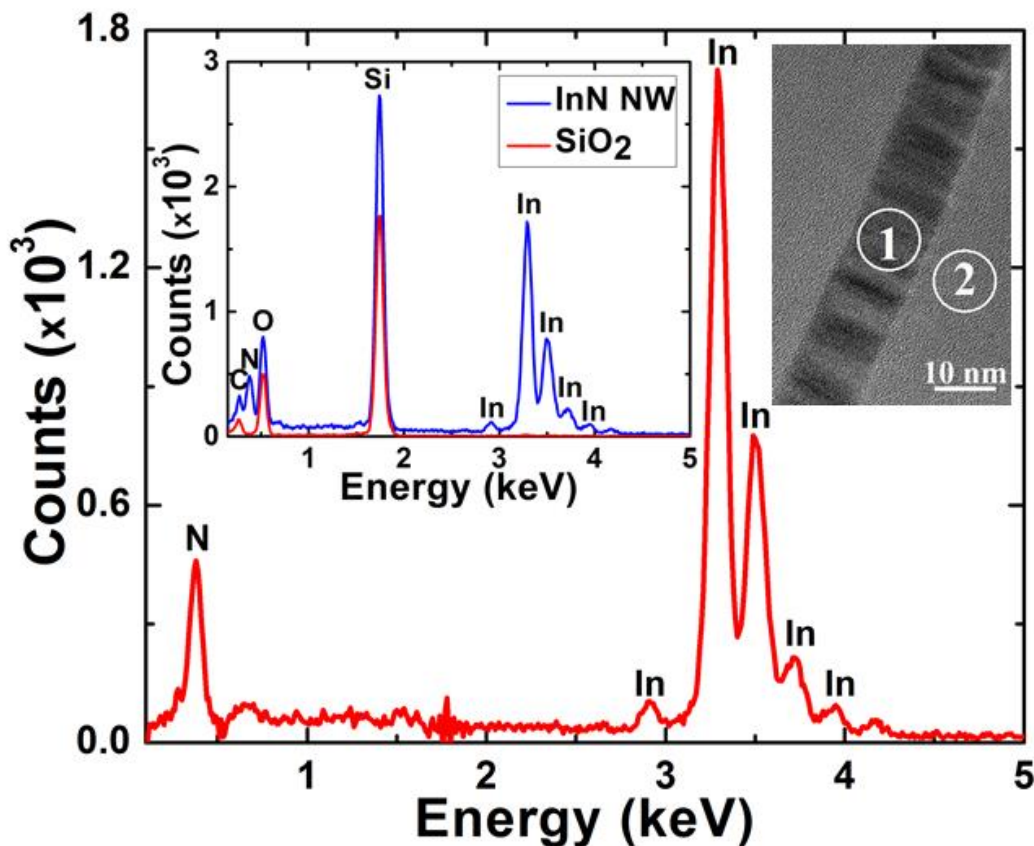

Figure 6.3 Adjusted EDS spectrum of a thin InN NW with contribution from SiO_2 membrane subtracted. Top left inset shows EDS spectra on InN NW and SiO_2 membrane. Top right inset shows TEM image with positions 1 and 2 where EDS spectra were taken.

6.2 Fabrication of Graphene/InN NW Heterojunction

Optical lithography (mask aligner Karl Suss MJB3) was used for fabricating InN NW/graphene heterostructures. The samples used here were square pieces taken from a 100 nm dry thermal SiO_2 on 500 μm Si wafer. After RCA and organic cleaning, the sample was first coated with lift-off resist (LOR3A) at 5000 rpm and baked at 150 ^{o}C for 1 minute. Then it was coated with negative resist NR71-3000P. A pe-exposure bake of 150 ^{o}C was used to remove any remaining solvent from the resist. The sample was then placed under the UV light using a bright field mask and exposed with a total dose of 280 mJ/cm^2. After exposure the sample was baked again at 100 ^{o}C, followed by development

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in RD-6 for about a minute or until the patterns were fully developed. E-beam evaporation method was used to depost a 2 nm thick layer of Au, followed by lift off in resist remover RR41 and subsequent organic cleaning.

Following the lift-off procedure, InN NWs were grown using the method described earlier. At optical image of the NWs growing out of the catalysts are shown in Figure 6.4.

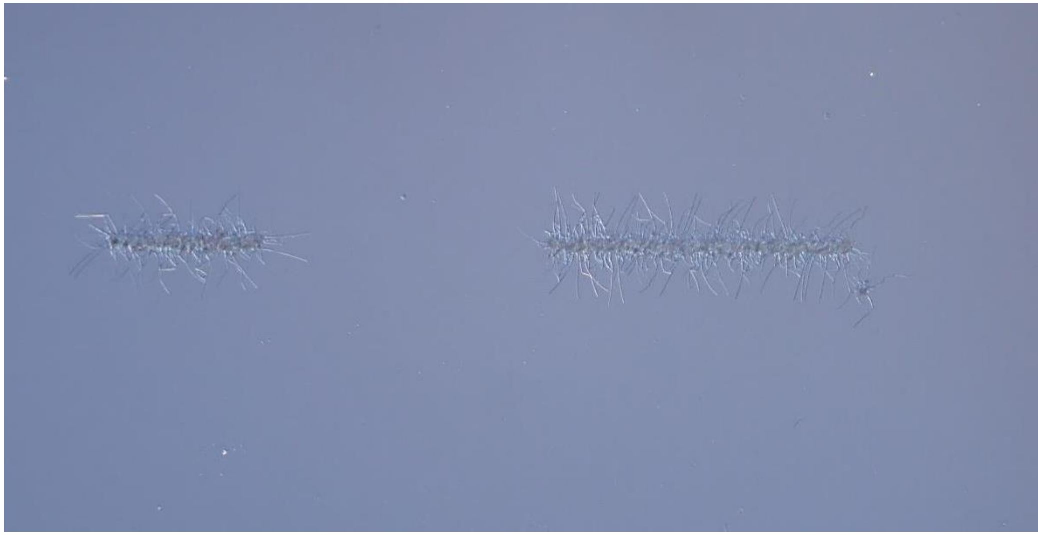

Figure 6.4 InN NWs grown out of 2 nm Au catalyst (catalyst pattern dimensions: 5 µm x 100 µm and 5 µm x 200 µm).

After the growth, a similar fabrication method was used to form extended metal contacts of 20/80 nm Ti/Au for NWs andd graphene. The open windows after development of the resist can be shown in Figure 6.5 (a), where NWs are seen at the upper edge of two windows (second row from the bottom). The final contacts can be seen in Figure 6.5(b) after the lift-off process. After that, we washed the NW samples in dilute HCl solution to remove any native oxide (In_2O_3) form the NW surface, followed by rinses in DI water. Graphene was immediately transferred on to the sample using the method described in Chapter 4. Another round of optical lithography was performed to

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pattern graphene, this time LOR3A and a positive resist (AZ1518) was used with a bright field mask, the recipe can be found in Appendix A.

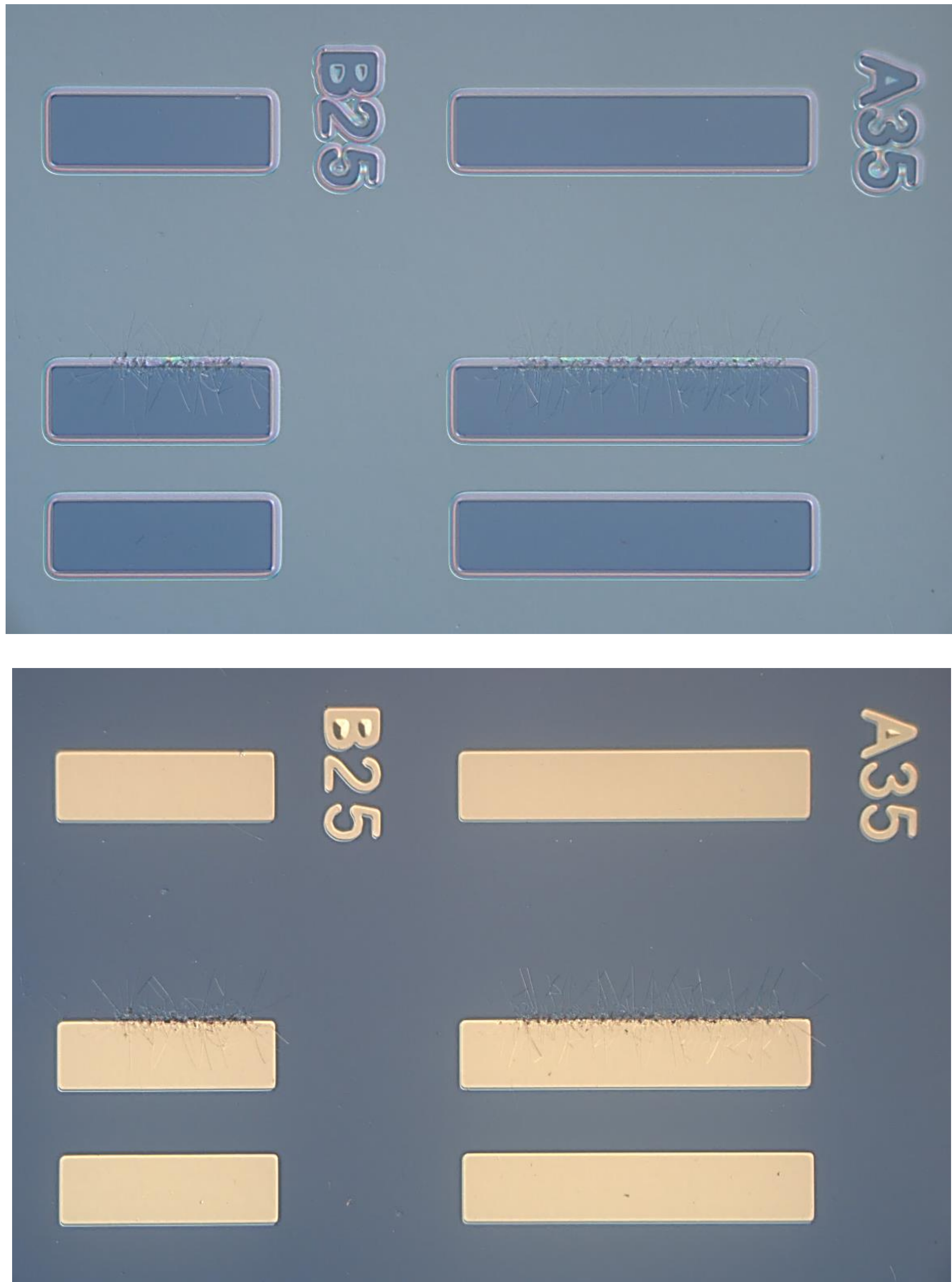

Figure 6.5 Optical microscope images of (top) photoresist pattern of metal contacts after development and (bottom) 20nm/80nm Ti/Au metal contacts deposited using e-beam evaporator.

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This process left rectangular patches of photoresist on graphene to protect it only on those places, while the rest of the graphene would be etched away. The discontinuity of the graphene patches would ensure the isolation of the resulting devices from each other.

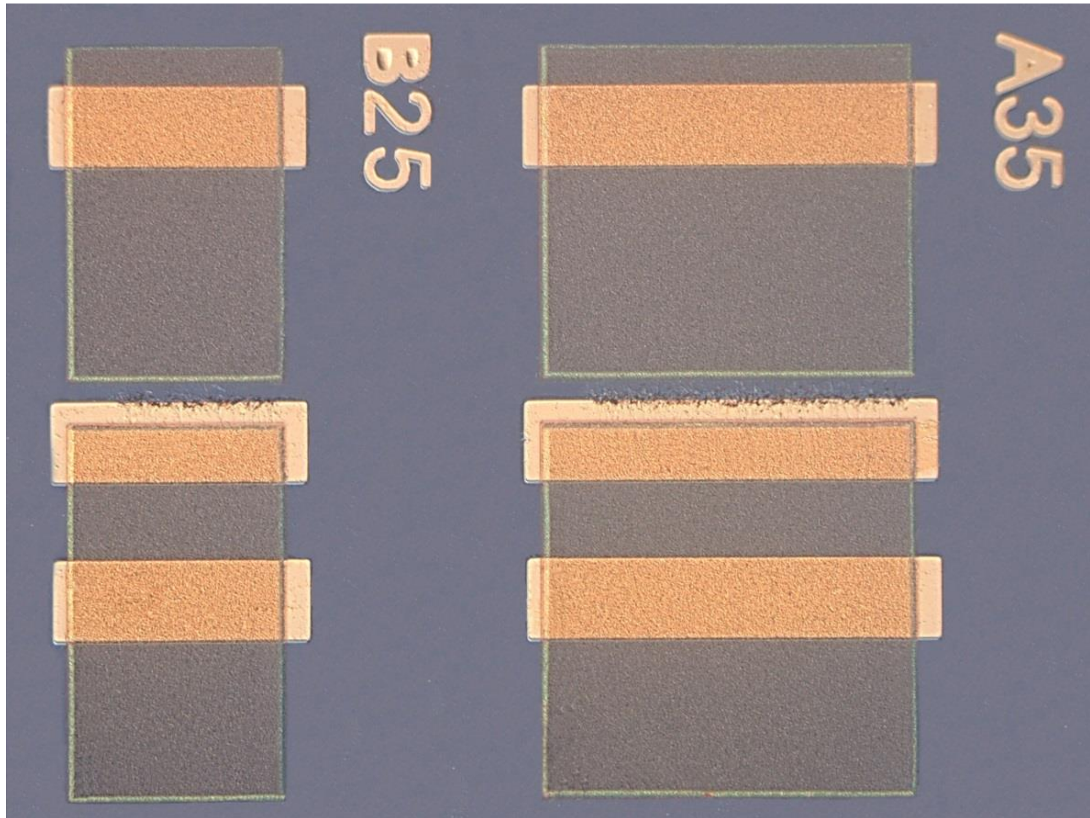

Figure 6.6 Optical image of patterned photoresist on graphene.

The sample was then placed in the RIE chamber and was exposed to O_2 plasma for 3 minutes, the result is shown in Figure 6.6, where we can see that the areas outside the resist are clean and the graphene was etched. The sample was then submerged in resist remove Mircoposit 1165 to remove the photoresist and LOR3A. Although this is not a lift-off process, we still used LOR because AZ1516 is very sensitive to O_2 plasma, and removing it after a plasma exposure can be very difficult. The introduction of LOR beneath it alleviates that problem. The final devices are shown in Figure 6.7.

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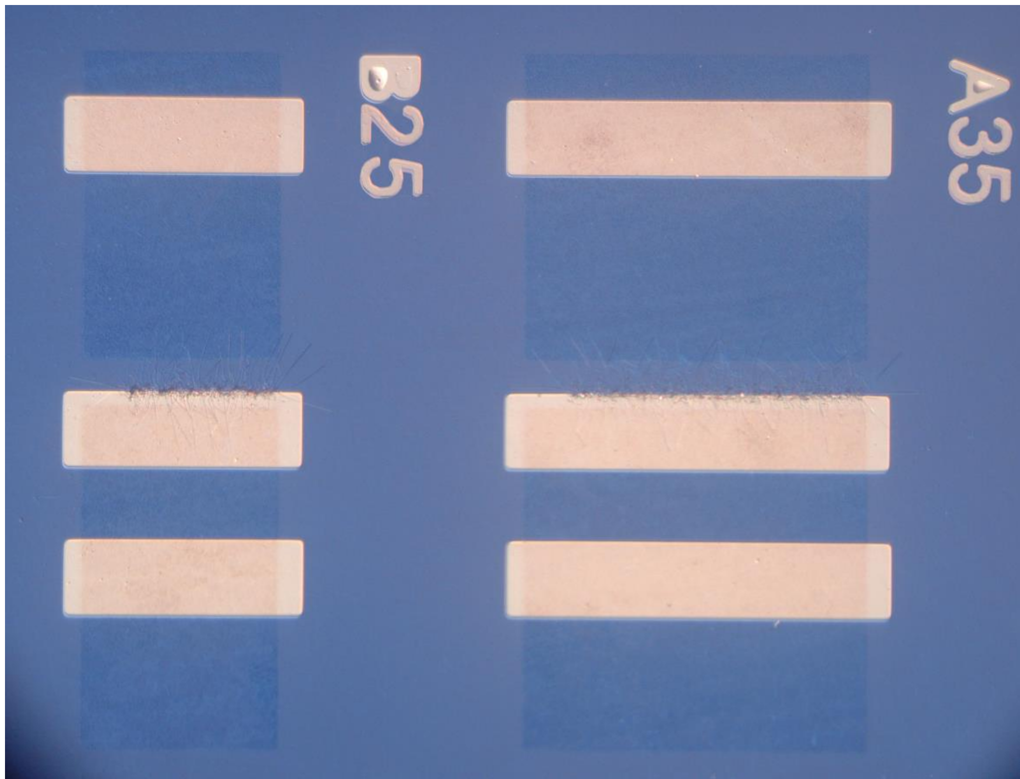

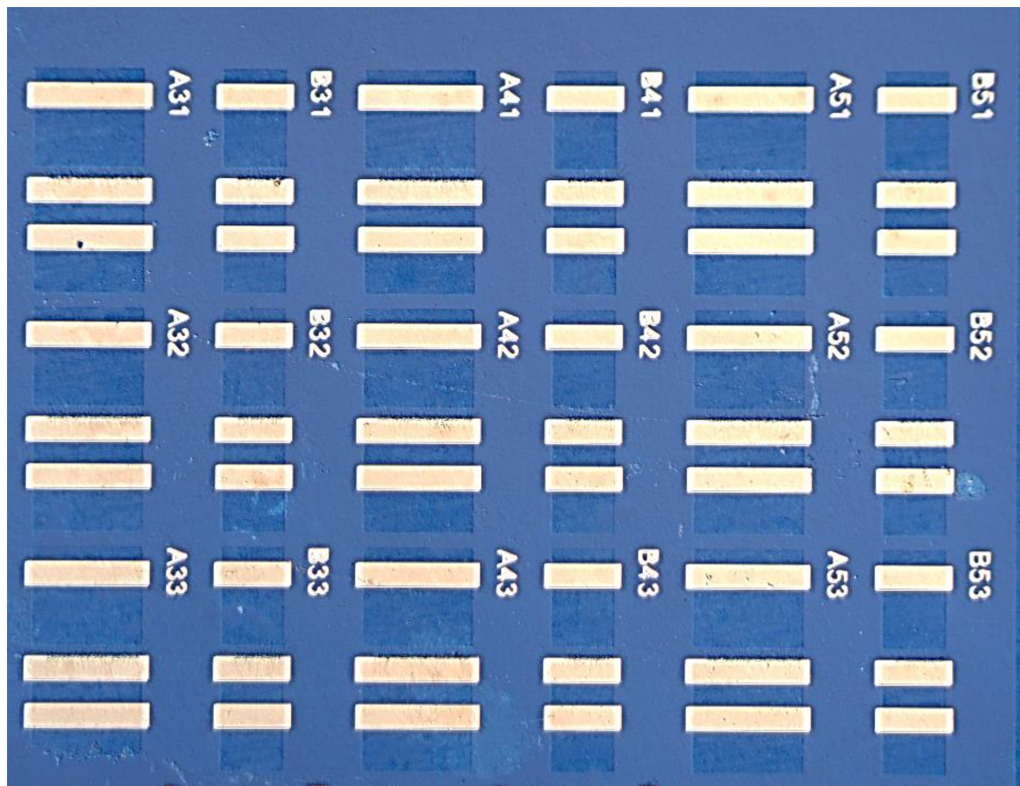

Figure 6.7 Optical images of (top) 2 devices and (bottom) multiple devices, after graphene transfer, graphene etch and resist removal.

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6.3 Characterization of Graphene/InN NW Heterojunction

The current-voltage measurements were performed using a Keithley 2612A System Source Meter unit. The schematic of the device is shown in Figure 6.8. Here we see that there are two contacts on graphene to study the electrical properties of graphene individually. The left contact on graphene (Figure 6.8) and the one on the other side of the heterojunction are the two required contacts for the heterojunction. Since the device is formed on n^+ Si substrate with a 100 nm thick dry thermal oxide (the same kind of substrate used for the graphene/MoS_2 barristor), it is possible to use this device in three-terminal mode. In a slightly different design (not shown here), we also have two very closely placed contacts on NWs, just like the two contacts we have here on graphene. That configuration is useful to study the behavior of the NWs, but that discussion is beyond the scope of this dissertation.

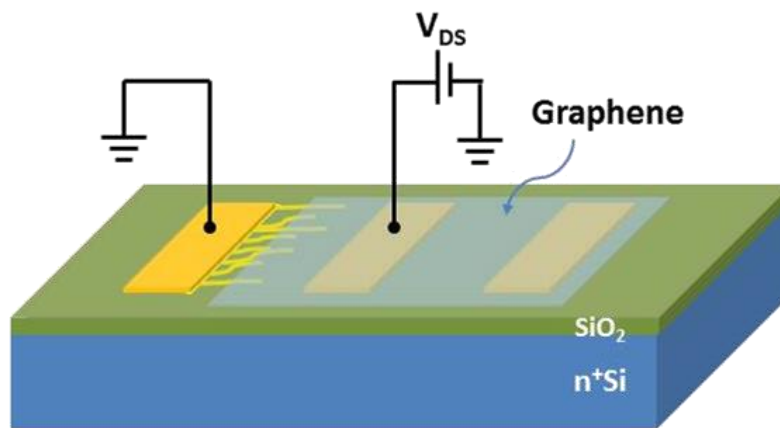

Figure 6.8 The schematic of the graphene/InN NW device. The existence of n^+ Si backgate allows this device to be used as a three terminal transistor device.

In Figure 6.9, we show the I-V characteristics of the pristine and modified graphene/InN NW heterojunction devices. The pristine InN NW-based device (indicated by “Pr-InN”) exhibits a slightly nonlinear ohmic behavior with very high current driving capacity. This high conductivity can be attributed to the very high surface charge

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accumulation of InN, which allows an ohmic contact to be formed. We attempted to alleviate this problem by passivating the surface with a thin layer of oxide. The most successful method was growing a thin layer of native oxide (In_2O_3) using O_2 plasma, this not only pasivates the dangling bonds at the surface, but also forms an interfacial tunnel barrier. In the subsequent discussion and their associated figures, we will use the term "Pr-InN" to refer to the pristine InN NW-based graphene/InN NW heterojunction (often abbreviated as "Gr/InN NW"). The term "OP-X", abbreviation of "**O**$_2$ **P**lasma - **X** minutes" with X being a non-zero integer, refers to the same kind of heterojunction where the NWs were treated by the O_2 plasma for X minutes. This treatment was performed before graphene transfer and the HCl rinse was omitted for these samples to prevent the removal of the oxide layer. All plasma treatment sessions were performed at 300 mtorr pressure and 150 W plasma power. Figure 6.9 shows a direct comparison in OP-X Gr/InN NW devices with the Pr-InN variant, where a longer plasma treatment results in a more pronounced Schottky behavior. The ideality factor (η) improves slightly with oxidation, with $\eta \approx 3.7$ for OP-1 and $\eta \approx 3.2$ for OP-5. The barrier height also increases significantly, which will be discussed later in Figure 6.12.

In Figure 6.10, the I_D-V_{DS} family of curves is shown for OP-5 Gr/InN NW device. The modulation of drain current and the subsequent change in barrier height is clearly obvious here, with a more negative gate bias reducing the current by increasing the barrier height. This is further clarified in the transfer curves of the Pr-InN and OP-5 based Gr/InN NWs at $V_{DS} = 5$ V, as shown in Figure 6.11, where we see a sharper change in the OP-5 Gr/InN NW device as V_{BG} varied. At around $V_{BG} = -8$ V the slope of the log(I_D) vs V_{BG} curve is maximum for OP-5, making it a favorable bias point for most of the sensing

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experiments that we performed later on.

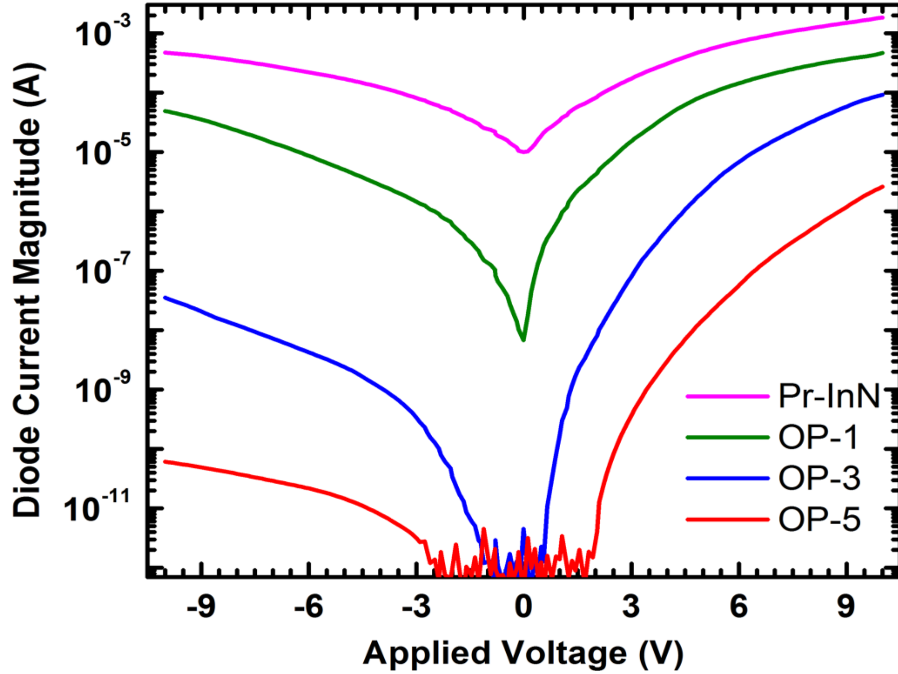

Figure 6.9 The I-V characteristics of Gr/InN NW heterojunction at zero gate bias. The samples had NWs with different plasma treatment durations.

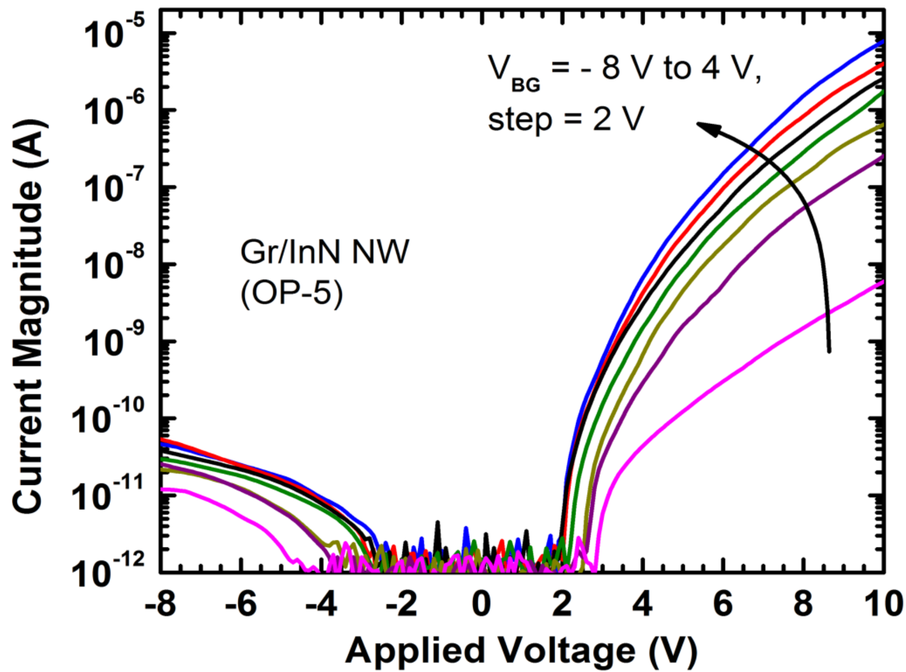

Figure 6.10 The effect of back-gate bias (V_{BG}) on the drain current for Gr/InN NW (OP-5) barristor device.

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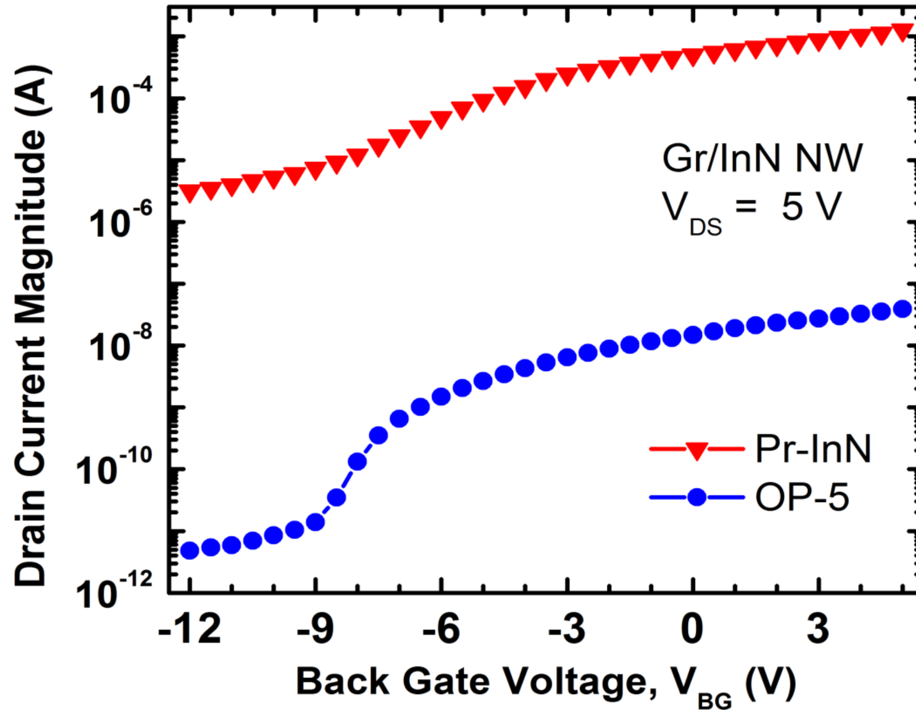

Figure 6.11 The transfer characteristics of two Gr/InN NW barristors (Pr-InN and OP-5) at $V_{DS} = 5$ V.

We can obtain the effective Schottky barrier height (SBH) using the thermionic emission model (equations (4)-(6), Section 4.2), however it should be noted that here we have an interfacial oxide layer which will require a tunneling mechanism to be incorporated in the model. This interfacial oxide layer causes a reduction in current by increasing the effective SBH and ideality factor (η). A factor, $\exp(-\alpha_T\sqrt{\varsigma}\delta)$, accounting for the suppression of the junction current due to the tunneling probability is incorporated in the expression of I_0 (reverse saturation current), where α_T (in $eV^{-0.5}\cdot Å^{-1}$) is a dimensional constant which depends on the effective mass m*; ς (in eV) and δ (in Å) are the barrier height and the thickness of the oxide layer respectively.[5] The modified expression of current density J (from equation (5)) is as follows:

$$J = J_0 \exp\left(-\alpha_T\sqrt{\varsigma}\delta\right)\left[\exp\left(\frac{qV}{\eta k_B T}\right) - 1\right] \qquad (8)$$

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In many cases, α_T is ignored because of its value often getting close to unity, such as ref. [4]. The overall reduction in current causes the ideality factor to get worse (i.e. increase in value), which is the case here as we have observed even the best value η to stay well above 2 for all our measurements. The tunneling related term cannot be accurately predicted here, due to the exact thickness of the barrier being unknown, the SBH can be estimated by noting the band offset between InN and In_2O_3. However, tunneling is not the only factor here that is responsible for the change in I_D after oxidation, the suppression of dangling bonds also plays an important role. The overall reduction in surface carrier concentration reduces the maximum electric field at the heterojunction interface, which lowers the image force that plays a significant part in barrier height lowering in Pr-InN based Gr/InN NW heterojunction. The variation of SBH with oxidation and V_{BG} is shown in Figure 6.12. From Pr-InN to OP-5, the SBH changed by over 1 eV for any V_{BG}, while a more negative V_{BG} caused the SBH to go up even more. This can be explained by image force incduced barrier lowering. At V_{BG} = -8 V, the NWs have a significantly low carrier concentration. As V_{BG} shifts towards more positive gate bias steps, the carrier concentration increases, which in turn lowers the SBH by image force induced barrier reduction. It is possible that at OP-1, reduction of surface states may be the dominant mechanism behind the increase of barrier height; while the tunneling mechaism may take over after a longer oxidation phase (~ OP-3 or OP-5), resulting in a significant increase in barrier height as shown in Figure 6.12. This explanation is based on Figure 6.13, where we see the EDX spectra of an OP-4 InN with distinct peaks for O and N. Inset shows how these two peak intensities vary from Pr-InN to OP-5; the N peak gradually goes down while the O peak goes up, indicating the NW surface becoming

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more O-rich with the increase of plasma duration.

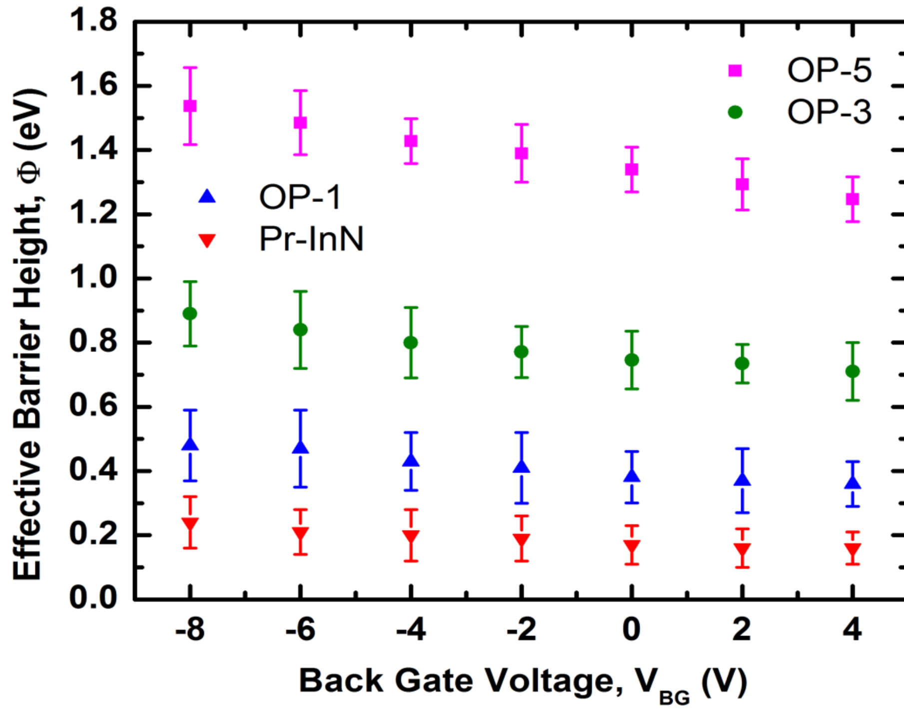

Figure 6.12 The variation of barrier height with different V_{BG} and plasma dosages, obtained using thermionic emission model with special considerations for tunneling.

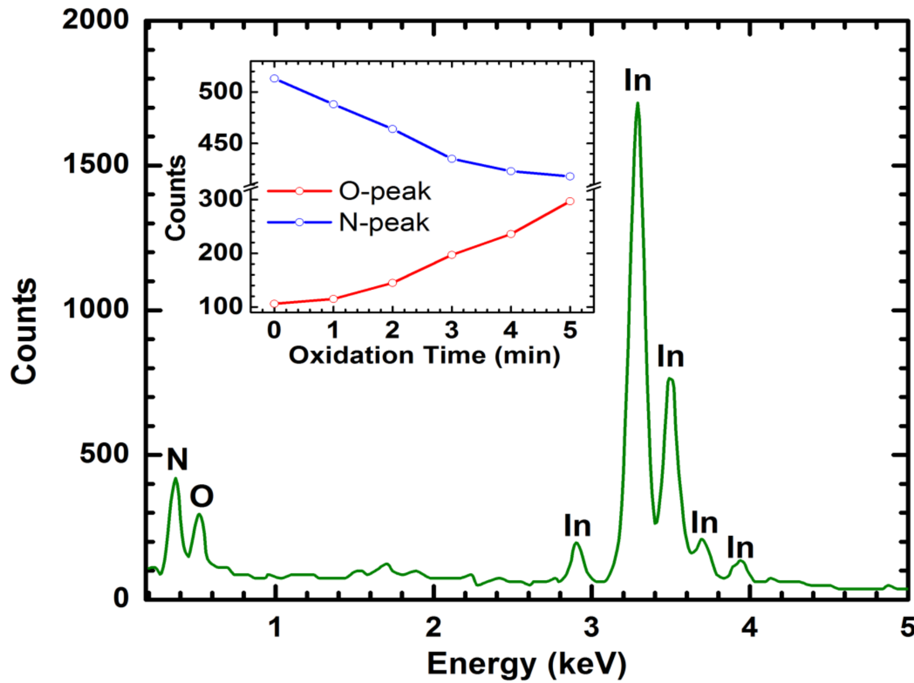

Figure 6.13 The EDX spectra of an OP-4 InN NW. Inset shows the variation of O and N peaks with plasma oxidation time.

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6.4 Detection of Trace Gases Using Graphene/InN NW Barristor

In this study, we exposed the device to a predetermined concentration of a toxic gas, such as NO_2, NH_3 or CO in a closed chamber and measured the change in resistance ($\Delta R/R_0$) in percentage. Due to the wide variation of I-V curves (e.g. SBH) with oxidation time and back gate voltage, it was not possible to keep the drain bias fixed for all measurements. Hence, an initial current value of 50 pA was arbitrarily defined, for each measurement the drain bias was set accordingly to achieve this initial current level. However, this was not a constant current experiment, the reference current level was used only to set the constant drain bias voltage for the sensing experiments.

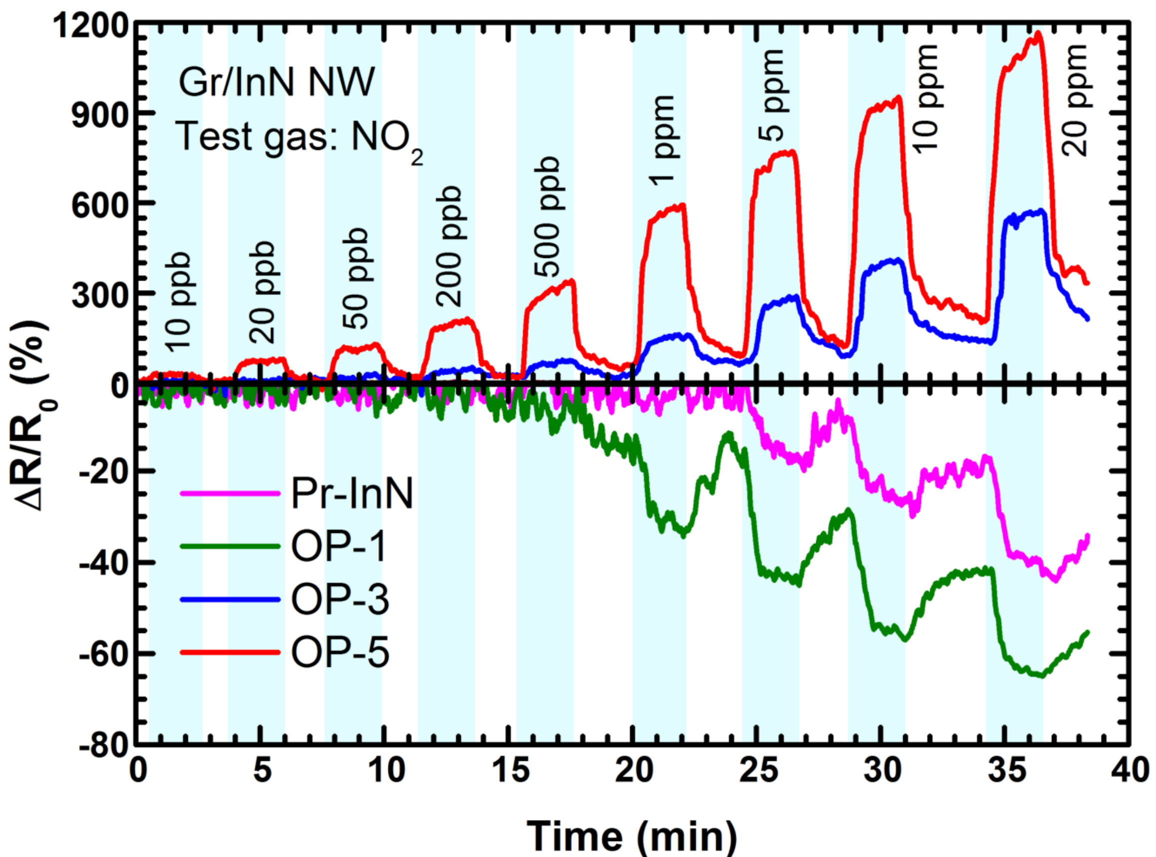

Figure 6.14 Composite plot showing the response ($\Delta R/R_0$ %) of the Pr-InN and OP-X based Gr/InN NW devices to different concentrations of NO_2 at $V_{BG} = 0$ V and $I_0 \approx 50$ pA.

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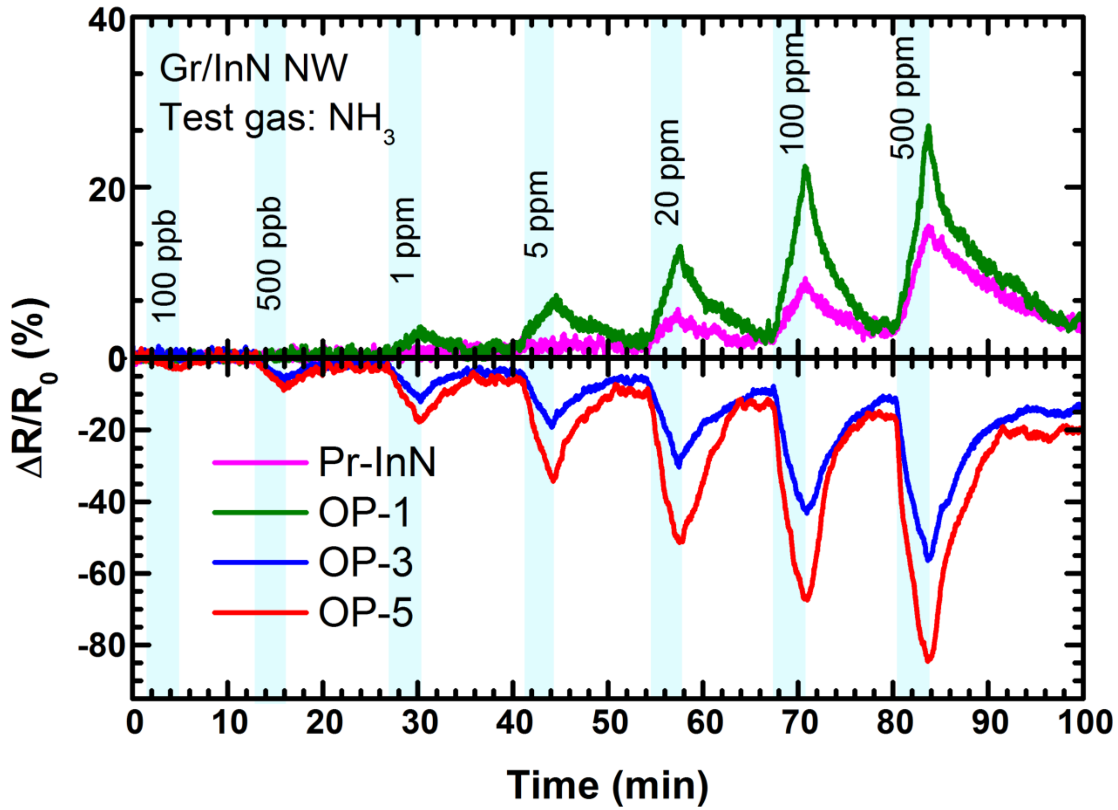

Figure 6.15 Composite plot showing the response ($\Delta R/R_0$ %) of the Pr-InN and OP-X based Gr/InN NW devices to different concentrations of NH_3 at $V_{BG} = 0$ V, $I_0 \approx 50$ pA.

In Figures Figure 6.14-Figure 6.16, we show the composite plots of $\Delta R/R_0$ in presence of NO_2, NH_3 and CO respectively, various Gr/InN NW barristor devices at $V_{BG} = 0$ V and $I_0 \approx 50$ pA. The nature of the response varied, depending on the NWs being used: Pr-InN, OP-1, OP-3 and OP-5. It is known that NO_2 is a moderately strong acceptor for graphene, while NH_3 and CO are both weak donors, CO being weaker than NH_3.[6]-[7] However, in Figure 6.14, we see opposing trends in the responses of Pr-InN, OP-1 and OP-3, OP-5. Since Pr-InN and OP-1 based devices were completely ohmic and nonlinearly ohmic respectively, we argue that in these two devices only graphene was dominating the sensing response and InN NWs were merely acting as non-rectifying contacts. Therefore, the shifting of the Dirac point of graphene, due to the introduction of NO_2, had no significant effect on the SBH, at least not enough to offset graphene's own

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response to NO_2. However, it is still not clear why OP-1 had a greater response to NO_2 (and also NH_3 and CO in the following discussion) compared to Pr-InN, further investigation is needed to understand this phenomenon. On the other hand, OP-3 and OP-5 had the opposite responses to NO_2 with, which is indicative of a diode-like action. Since NO_2 is an acceptor, it moves the Dirac point towards the valence band of graphene which allows the effective SBH between graphene and InN to decrease. This increases the current and decreases the resistance, as seen in Figure 6.14.

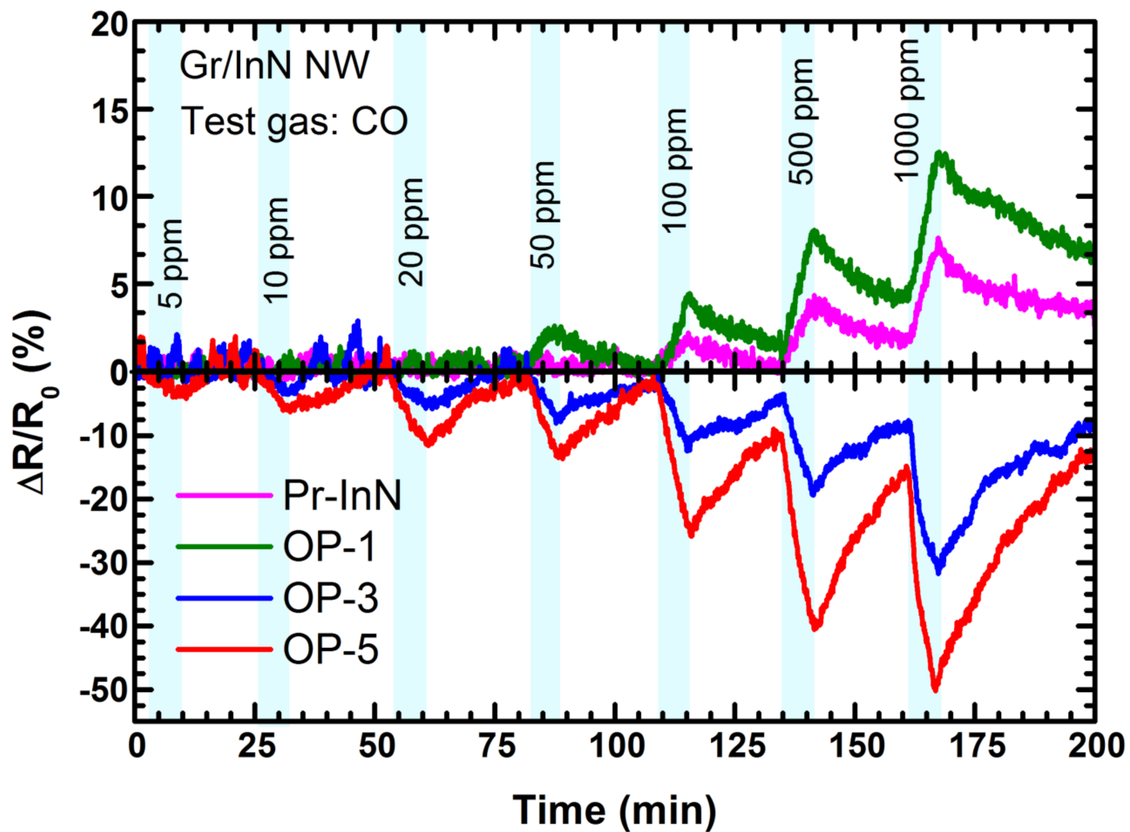

Figure 6.16 Composite plot showing the response ($\Delta R/R_0$ %) of the Pr-InN and OP-X based Gr/InN NW devices to different concentrations of CO at $V_{BG} = 0$ V and $I_0 \approx 50$ pA.

Since NH_3 and CO are weak donors, the aforementioned devices are expected to respond in the opposite direction when being exposed to them. This is what was observed, as shown in Figure 6.15 (NH_3) and Figure 6.16 (CO). In all the three cases, the OP-5

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based device performed the best, that is why we only investigated in the performance of this device throughout the rest of this section.

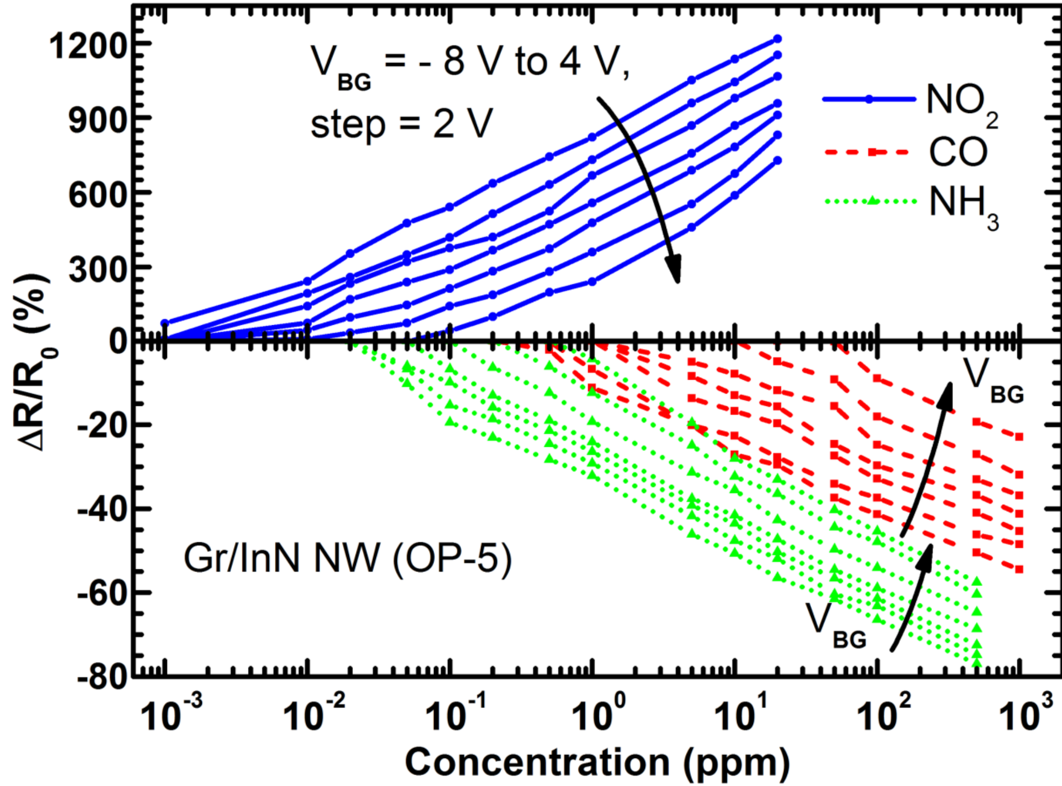

Figure 6.17 Composite plot showing the response ($\Delta R/R_0$ %) of the Pr-InN and OP-X based Gr/InN NW devices to different concentrations of NO_2, NH_3 and CO at different gate biases and $I_0 \approx 50$ pA.

Next, we studied the effect of V_{BG} on the response of the OP-5 barristor. In Figure 6.17, we see the $\Delta R/R_0$ for the OP-5 barristor at different V_{BG} and gas concentration. As V_{BG} becomes more negative, the response magnitude increases for all three gases, which can be attributed to the more pronounced Schottky behavior. The improved sensitivity also results in a lower limit of detection for each of these three gases, as shown in Figure 6.18. From this figure, we see that OP-5 barristor, at V_{BG} = -8V, has a noise limited lower limit od detection (LOD) of 0.5 ppb (parts per billion) for NO_2, 30 ppb for NH_3 and 300 ppb for CO.

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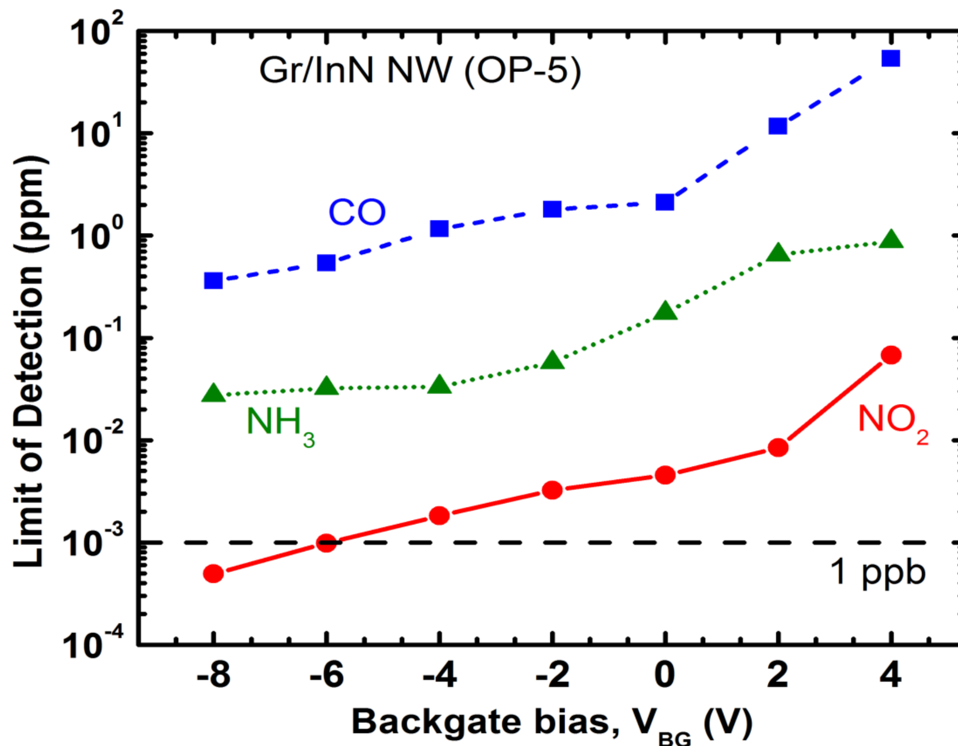

Figure 6.18 The limit of detection (ppm) of NO_2, NH_3 and CO, using an OP-5 barristor operating at different back gate biases.

From Figures Figure 6.14-Figure 6.18, we can draw the conclusion that the barristor action can improve the sensitivity and the detection limit of the Gr/InN NW heterojunction by more than an order of magnitude. We now focus on the selectivity of this sensor to particular analytes only. It is possible to functionalize the top surface of the barristor with specific chemical agents, one example being Fe-porphyrin (hemin), which is sensitive to NO and NO_2.[8]-[11]

Hemin-Cl was purchased commercially and was dissolved in 1-2 mM concentrations in dimethylformamide (DMF). Benzoic acid crystals were then added to the solution (5:1 ratio of benzoic acid to hemin) to aid in the surface functionalization action of hemin. After the solution was prepared, the fabricated barristor surfaces were cleaned in acetone, methanol and DI water and then dried with UHP N_2 gas. The samples were immersed into the hemin/benzoic acid solution for about 2 h, rinsed with a 5% v/v

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chloroform/hexane solution and then dried with UHP N_2 gas. The goal of this procedure was to obtain a uniform monolayer of dispersed hemin and benzoic acid molecules chemically attached onto the sample surface, as seen in Figure 6.19.

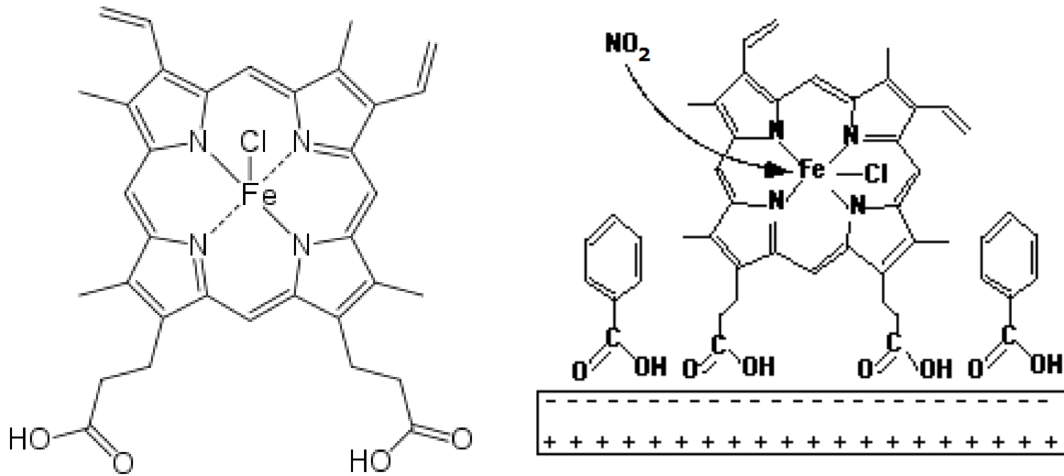

Figure 6.19 (Left) Chemical structure of Fe-porphyrin (hemin). (Right) Mechanism of hemin and benzoic acid molecules acting as a functionalization layer.

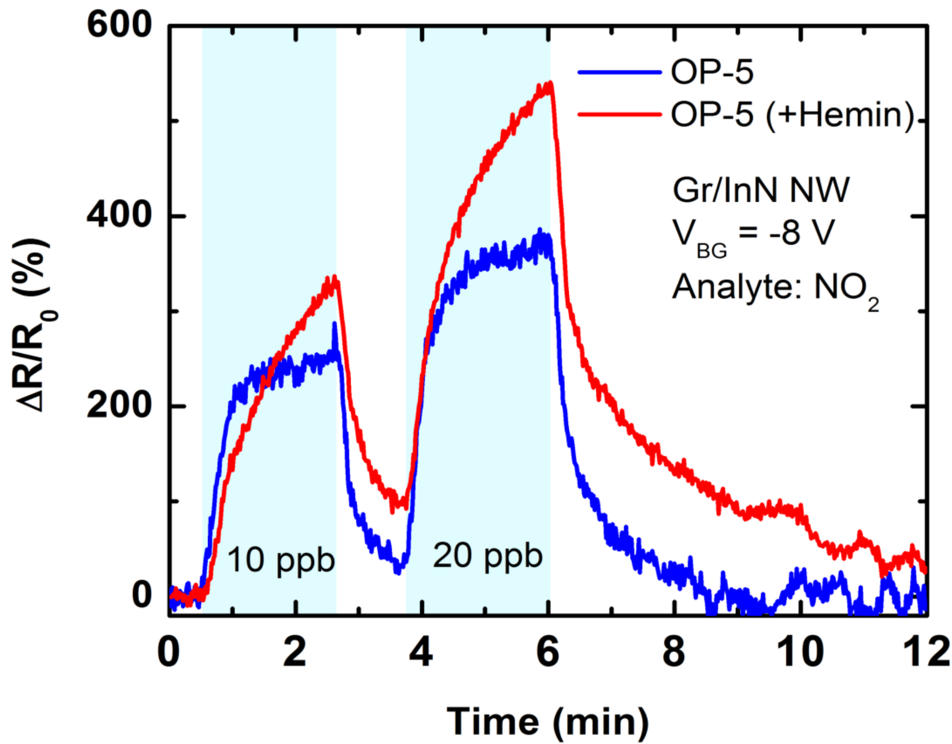

Figure 6.20 Response of an OP-5 barristor to NO_2 with and without Fe-porphyrin (hemin) functionalization.

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Figure 6.20 shows a comparison between two OP-5 barristors in presence of 10 and 20 ppb of NO_2, one with a bare surface and the other one with hemin/benzoic acid functionalization. The functionalizaed device was more sensitive compared to the bare one, though the rise/fall times were much larger for the functionalized device, which could be attributed to the modification of the surface energy upon introduction of the hemin/benzoic acid. Figure 6.21 shows the effective barrier heights calculated from the I-V curves taken with and without hemin on OP-5 barristor. Here we see that the functionalization layer increased the SBH by about 0.07 eV. The changes in SBH with NH_3 and CO were smaller than that with NO_2 for the bare device, but for the functionalized device those variations were even smaller. This indicates that the device may more readily respond to NO_2 than the other gases. Similarly, other types of functionalization layers can be used to improve the selectivity of the sensor.

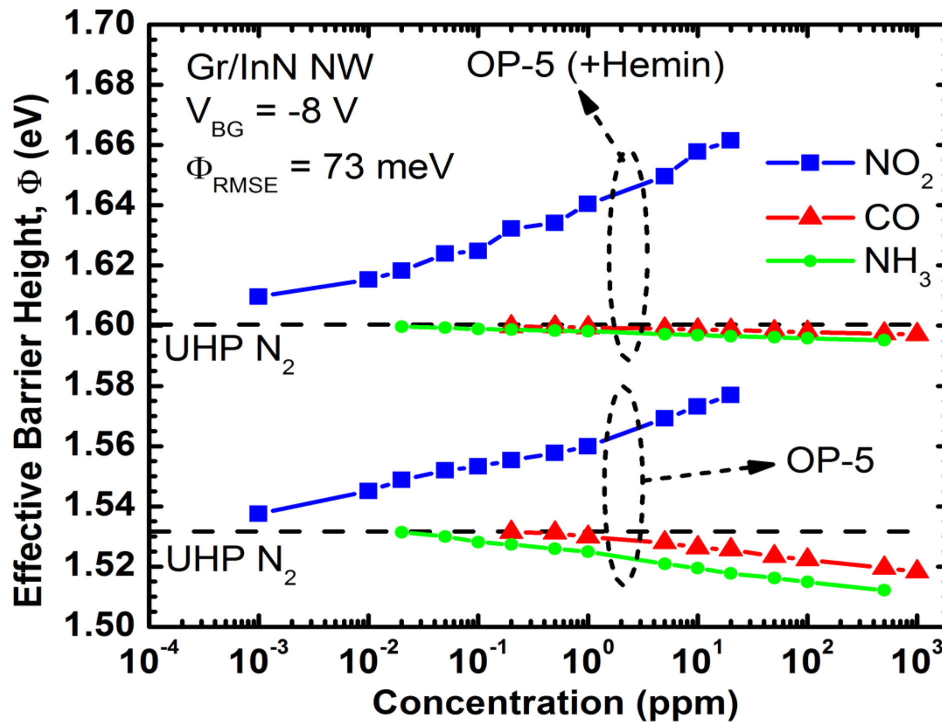

Figure 6.21 Effective barrier height in presence of various gases, calculated for OP-5 barristors with and without hemin/benzoic acid functionalization.

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6.5 Highly Sensitive Barristor Based Photo Detector

In this section, we present the optical response of the OP-5 barristor device. A Bosch & Lomb monochromator (wavelength range 300-800 nm) was used as the monochrome light source, which was focused on the device using different microscope objective lenses on a probe station. The incident power on the device was measured by using a commercial powermeter with spectral range of 200-1100 nm. At first, we chose 550 nm wavelength (greenish yellow) light for all optical measurements, followed by a spectral response analysis.

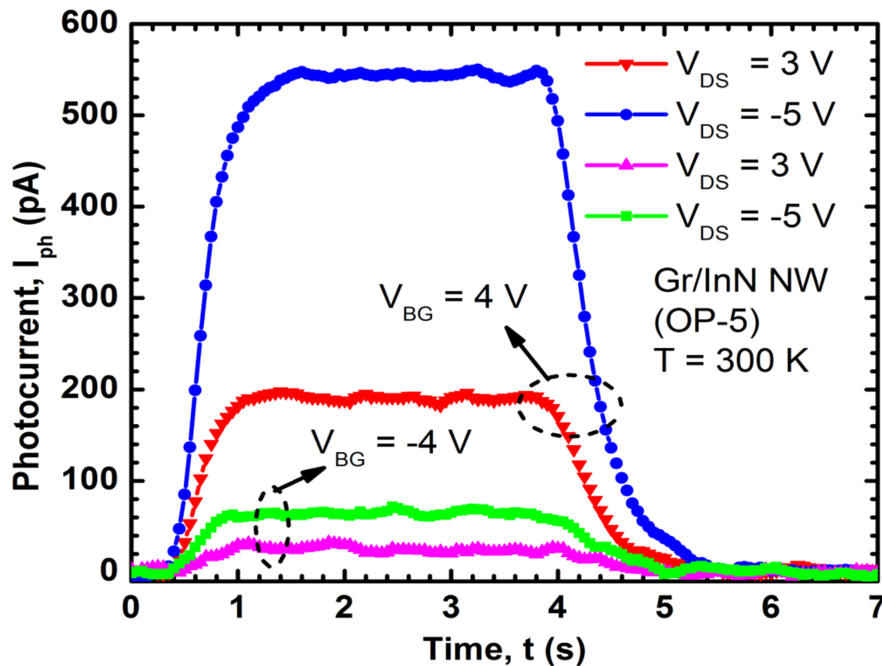

Figure 6.22 Time resolved photocurrent measurement at 550 nm wavelength (1 W/m^2), at 300 K.

In Figure 6.22, we see the time resolved photo response (photocurrent, I_{ph} = current under illumination – dark current) at room temperature and 550 nm wavelength (optical power, P_{opt} = 1W/m^2) using the OP-5 barristor. Four different drain-gate bias combinations were chosen. It is observed that a positive V_{BG} results in higher

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photocurrents, due to the lower barrier that allows more photocarriers to pass through before recombining. On the other hand, a negative drain bias (reverse biased junction) yields greater photocurrent because of the higher carrier extraction efficiency due to the electric field quickly separating the generated EHPs (electron hole pairs) from each other. Figure 6.23 shows a similar result for T = 200 K, where lower photocurrents are observed due to the lower rate of thermal generation. We have repeated the experiment for various optical powers from 1 mW/m^2 to 100 W/m^2 and recorded the photocurrent for all four bias configurations (Figure 6.24).

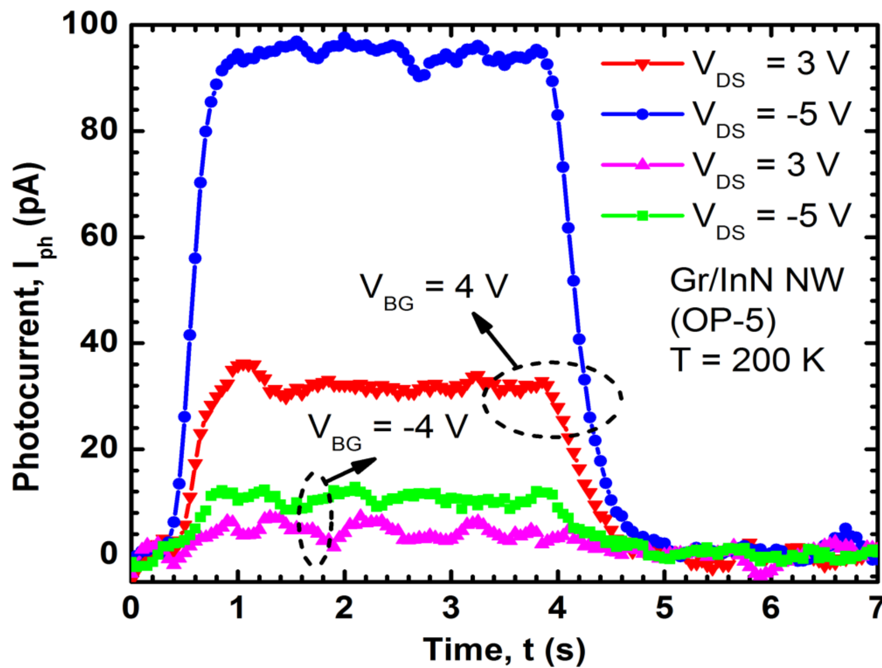

Figure 6.23 Time resolved photocurrent measurement at 550 nm wavelength (1 W/m^2), at 200 K.

In Figure 6.22, we see the time resolved photo response (photocurrent =current under illumination – dark current) at room temperature using the OP-5 barristor. Four different drain-gate bias combinations were chosen. It is observed that a positive V_{BG} results in higher photocurrents, due to the lower barrier that allows more photocarriers to pass through before recombining. On the other hand, a negative drain bias (reverse biased

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junction) yields greater photocurrent because of the higher carrier extraction efficiency due to the electric field quickly separating the generated EHPs (electron hole pairs) from each other. Figure 6.23 shows a similar result for T = 200 K, where lower photocurrents are observed due to the lower rate of thermal generation.

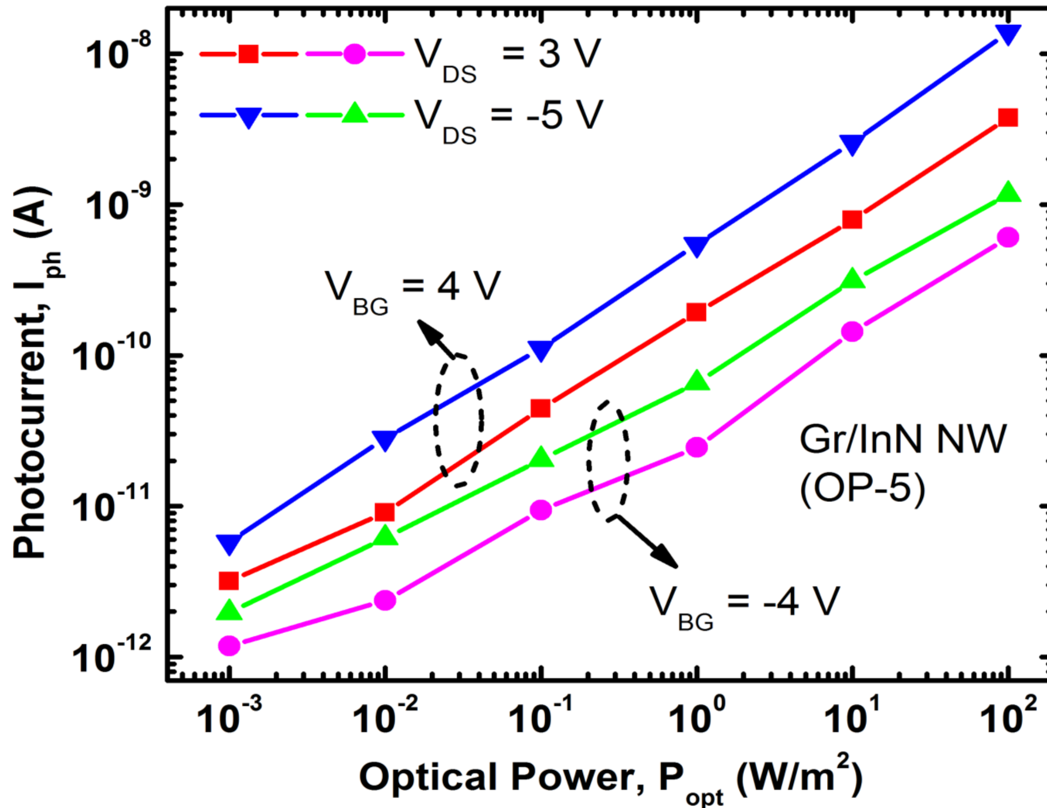

Figure 6.24 The photocurrent vs. optical power curves at different bias configurations, at 550 nm wavelength and 300 K.

From the data in Figure 6.24, we calculated the responsivity, $R_{opt} = I_{ph}/P_{opt}$ in A/W and presented it in Figure 6.25. A much higher R_{opt} was noted at low power regime, which gradually decreased as P_{opt} went up. Carrier concentration was found out to be inversely proportional to the device resistance × transconductance, using which the ratio of photo-generated carrier concentration to dark carrier concentration was determined and shown in Figure 6.26.

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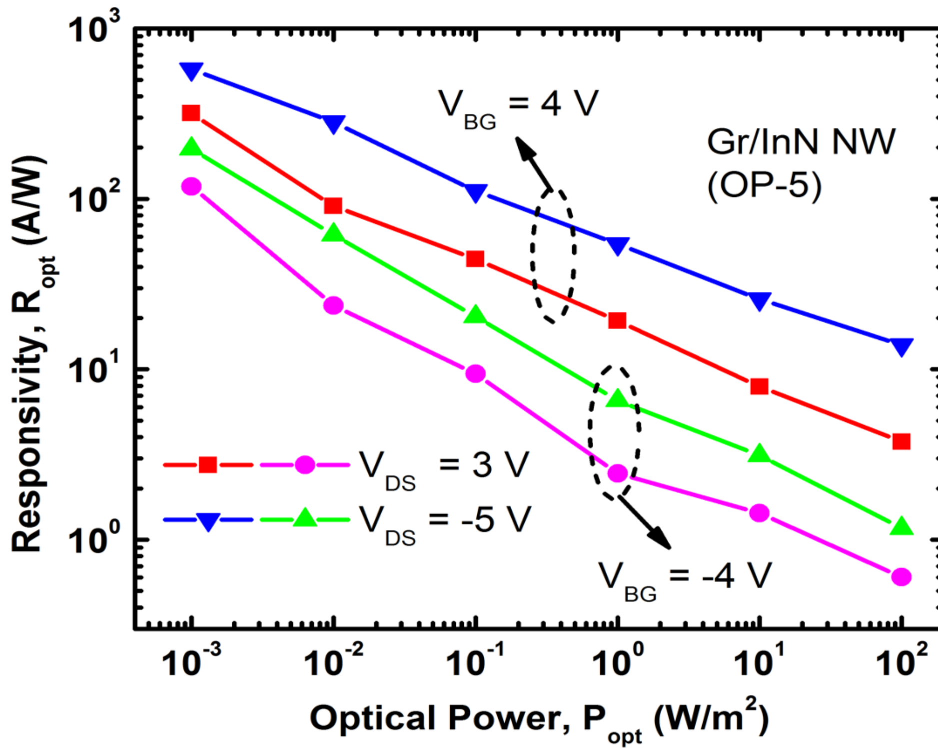

Figure 6.25 The responsivity vs. optical power curves at different bias configurations, from the same data as shown in Figure 6.24.

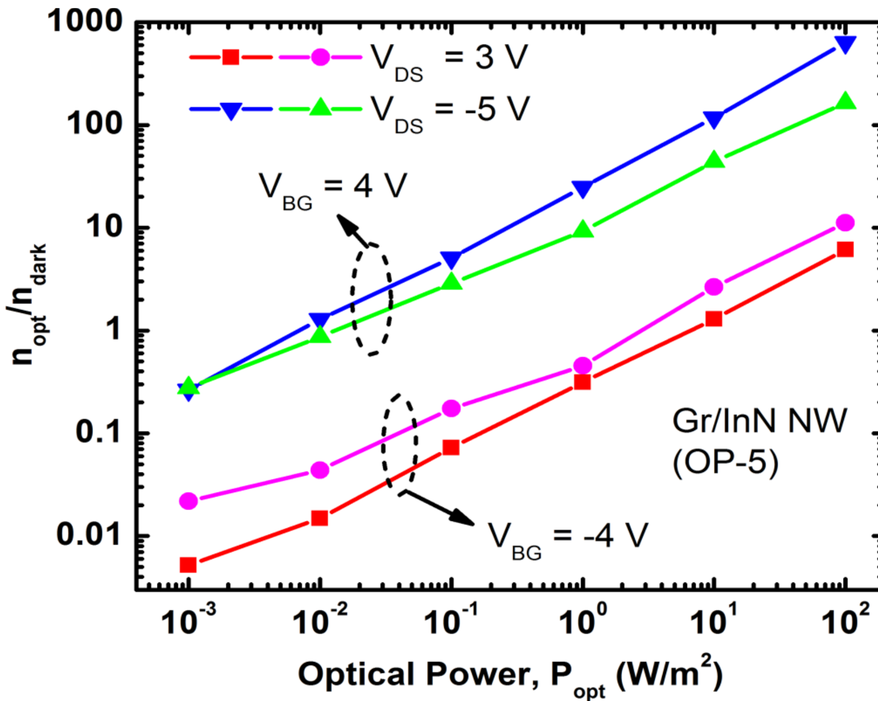

Figure 6.26 Ratio of photo-generated carrier and dark carrier concentration vs. optical power at different bias configurations, from the same data as shown in Figure 6.24.

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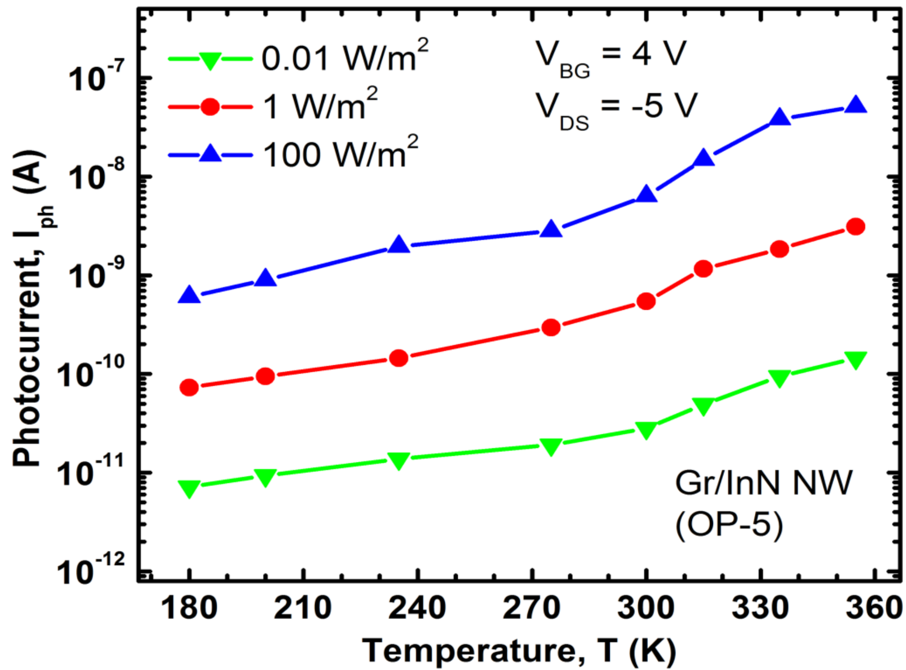

Figure 6.27 The photocurrent vs. temperature curves at different bias configurations, at 550 nm wavelength.

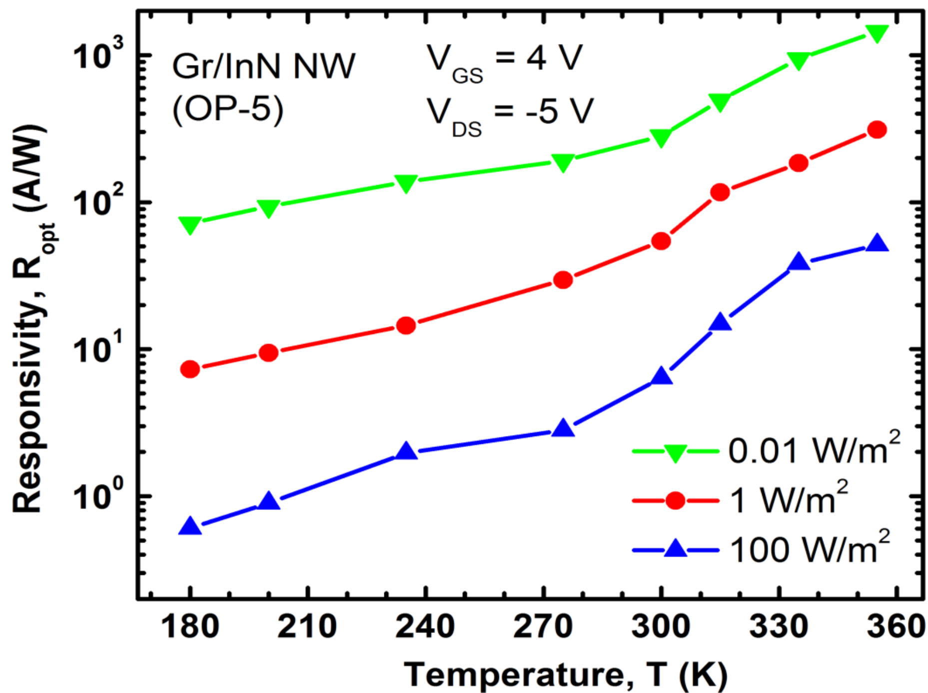

Figure 6.28 The photocurrent vs. temperature curves at different bias configurations, at 550 nm wavelength.

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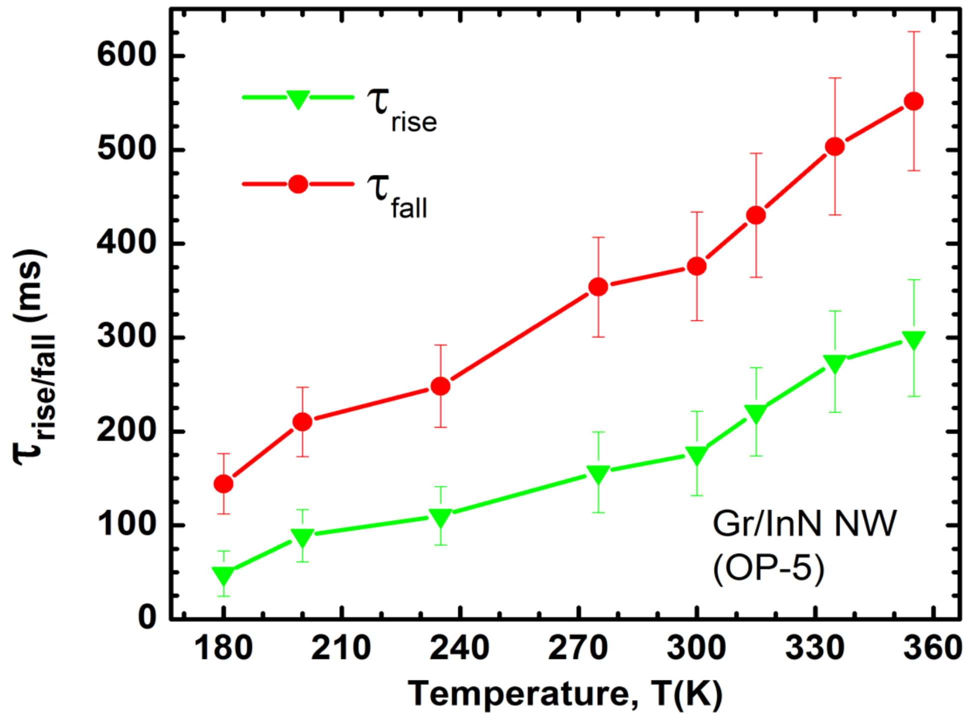

Figure 6.29 The response time constants for the OP-5 barristor device at 550 nm wavelength.

Similarly, the effect of temperature on photocurrent and responsivity are shown in Figure 6.27 and Figure 6.28 respectively. Figure 6.29 shows a compilation of all the rise and fall time constants vs. temperature, at 550 nm wavelength. The resistance of the barristor device was typically in 10^{9}-10^{12} Ω range (in operating condition), while the estimated junction capacitance was in 10^{-18}-10^{-15} F range. From this, we get the range of RC time constant as 10^{-9} -10^{-3} s. However, the measured time constant was at least 2-3 orders greater than that, which can be attributed to the trapping effect. Typically holes can get trapped, slowing down the recombination rate. This increases the photocurrent greatly as the photo-generated electrons may circulate through the system multiple times before recombining with the holes, increasing the responsivity at the expense of longer response time. The high responsivity can directly be associated with this photoconductive

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gain as well. As the temperature goes up, this gain increases, which causes the time constants to increase at higher temperature as well.

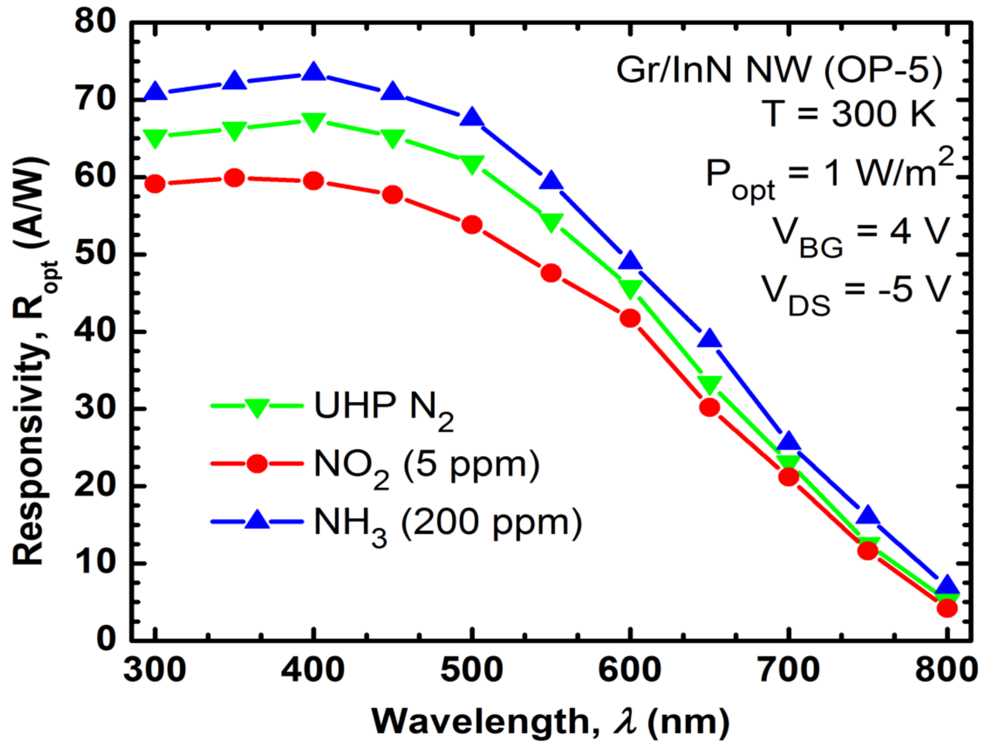

Figure 6.30 Spectral responsivity of the OP-5 barristor device at a fixed bias condition and $P_{opt} = 1$ W/m^2. The effect of molecular doping by gaseous species is also shown.

Figure 6.30 shows the spectral responsivity of the OP-5 barristor device. We chose the same bias configuration that yielded the best responsivity in the previous measurements for consistency. At a constant 1 W/m^2 optical power, the wavelength was varied from 300 nm to 800 nm as well. The responsivity starts to increase from 800 nm, reaches a maximum value at around 400 nm and the slightly decreases towards 300 nm. We also repeated the same experiment in presence of NO_2 and NH_3, which are known to modify the barrier height as seen in the previous section. The results were as expected, with NH_3 (lower barrier) the responsivity slightly increased while it slightly decreased with NO_2 (higher barrier).

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6.6 Gate Tunable Memristor

As we keep increasing the plasma duration, eventually the oxide starts to get thicker and the presence of oxygen vacancies become more likely. These vacancies can physically move as the current flows in one direction, changing the resistance with time. As the current is flown in the opposite direction, the vacancies start to return to their initial position, resetting the resistance to its initial state. Figure 6.31 shows a pinched hysteresis curve like that, in logarithmic scale, where three different gate voltages are used and the I-V loop appears to vary with V_{BG}. The device was an OP-8 barristor.

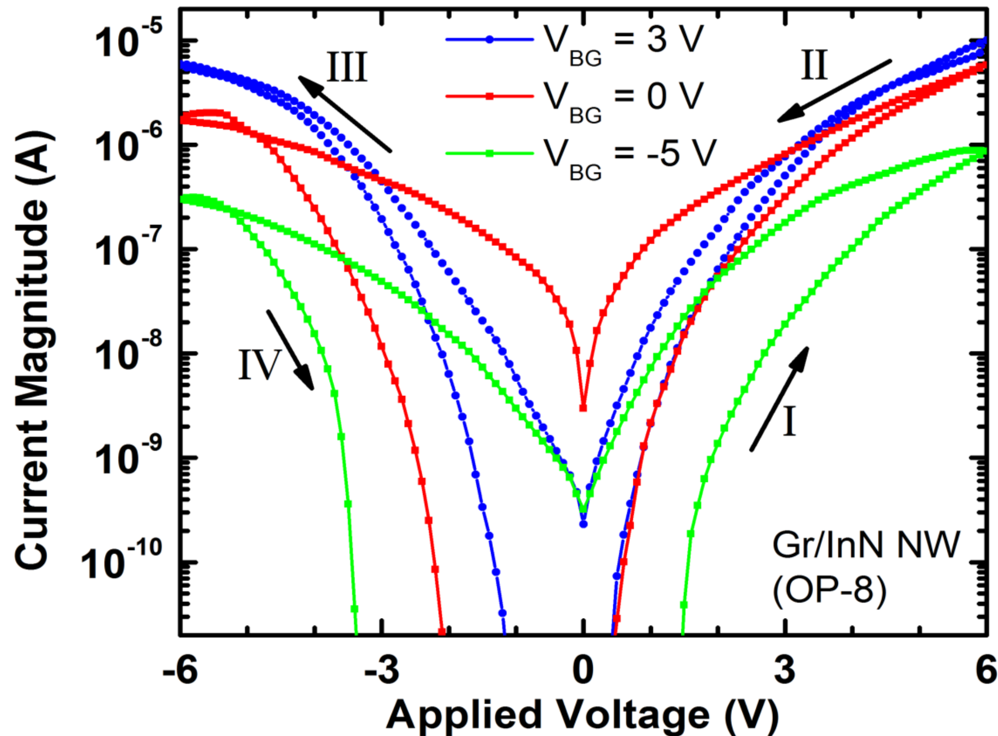

Figure 6.31 Pinched hysteresis curves obtained from OP-8 barristor at three different back gate biases.

The sweep direction is marked by roman numerals in Figure 6.31. In order to better understand the memristor action, we define two alternating resistors along the sweep direction. Arrows I and IV mark the low current path and the associated resistance

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is denoted by R_{high}. On the other hand, arrows II and III mark the high current path, with resistance denoted by R_{low}. In Figure 6.32, we plot the ratio R_{low}/R_{high} as a function of drain bias. Here we clearly see that R_{low}/R_{high} gradually decreases from the maximum V_{DS} on either direction, so the extent of the hysteresis can be related to the range of V_{DS} for which $R_{low}/R_{high} < 1$. For the sake of comparison, we define an arbitrary threshold value of $R_{low}/R_{high} < 0.1$, any voltage range satisfying this condition is marked as $\Delta V_{0.1}$. For example, if we consider the V_{BG} = -5 V curve, it crosees the dashed line at R_{low}/R_{high} = 0.1 twice, at around -3.75 V and around 3 V. This gives the total voltage range $\Delta V_{0.1}$ = 6.75 V for which $R_{low}/R_{high} < 0.1$. In Figure 6.33, we showed the effect of gate bias and temperture on $\Delta V_{0.1}$.

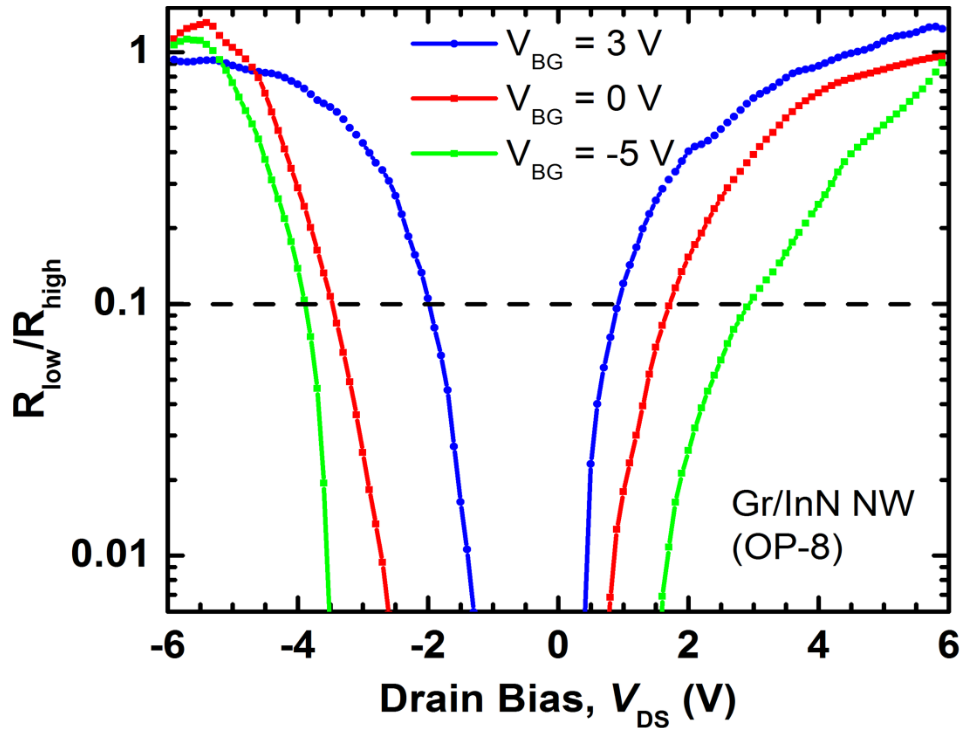

Figure 6.32 R_{low}/R_{high} vs. V_{DS} for three different V_{BG}.

As the gate bias becomes more negative, the InN gets more and more depleted, allowing some current to flow through In_2O_3 horizontally along the length of NW, at least

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for some distance. This can be better understood by considering InN/In_2O_3 core-shell NW as a resistive network, where InN used to form a shunt, confining the current through In_2O_3 to only in vertical direction. With further depletion, the InN can no longer act as a shunt as its resistance goes up, increasing the horizontal current in In_2O_3. The longer the current can flow through In_2O_3, the more it can affect the resistance, which is why at more negative V_{BG} the $\Delta V_{0.1}$ gradually increased. At higher temperature, the O-vacancies can move more quickly, allowing faster sweep time (Figure 6.34) and $\Delta V_{0.1}$.

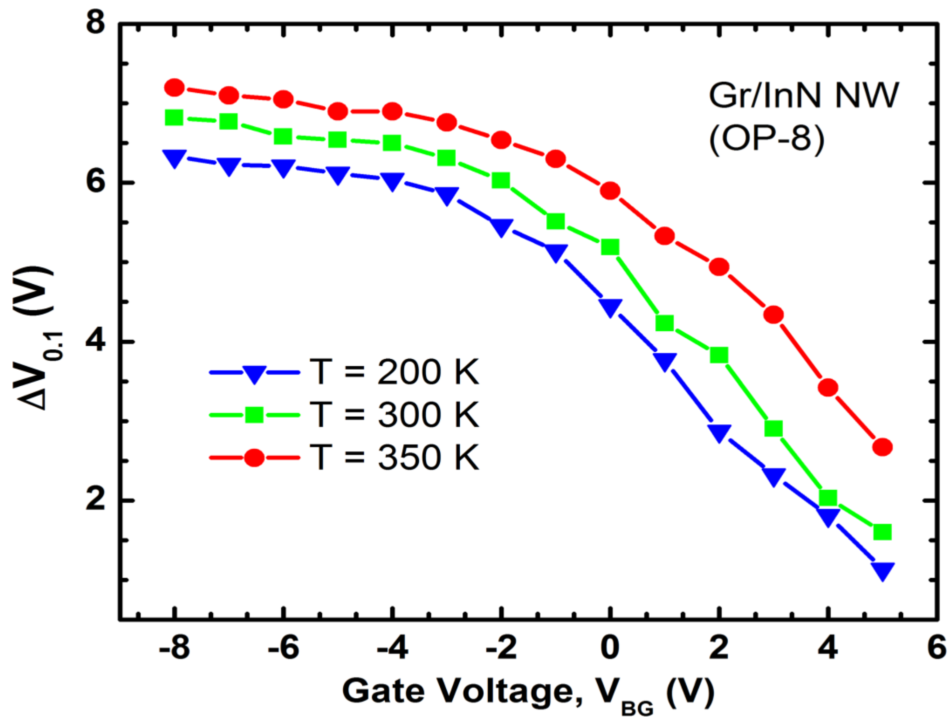

Figure 6.33 Effect of temperature and V_{BG} on $\Delta V_{0.1}$.

Finally, in Figure 6.34, we see the effect of sweep rate on $\Delta V_{0.1}$. As we keep increasing the sweep speed, the memristive property starts to diminish due to the slow movement of the O-vacancies. A negative V_{BG} allows the memristor device to keep up with a faster sweep rate. Figures Figure 6.33 and Figure 6.34 directly prove the gate tunability of the is novel memristor device.

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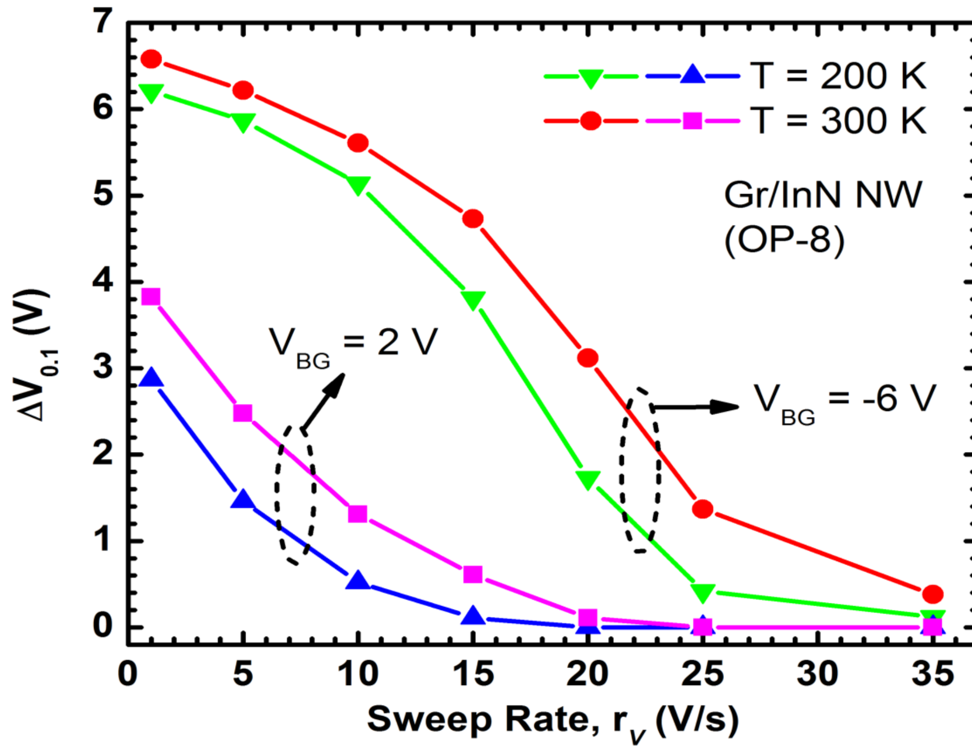

Figure 6.34 Effect of temperature and sweep rate on $\Delta V_{0.1}$.

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Chapter 7

Conclusion

7.1 Summary

In summary, we have demonstrated an improved growth technique for synthesizing top-down, large area, transfer-free 3-5 ML thick MoS_2 on SiO_2, reducing gate leakage by $>10^8$ compared to a longer duration, direct sulfidation method shown in this work. FETs fabricated from these layers were characterized in accumulation, depletion and inversion modes to study the complete transfer behavior, which showed a normally-on accumulation mode characteristics with $\mu_{FET} > 80$ cm^2/Vs, SS < 90 mV/decade, and ON/OFF ratio of $>10^5$. The observed temperature stability of FET metrics up to a temperature of 500 K is due to the canceling of ionized impurity scattering and phonon scattering. Asymmetry was observed between the accumulation and inversion modes, which were attributed to the metal/semiconductor Schottky junctions at the source/drain ends.

A graphene/MoS_2 barristor on an n^+ Si/SiO_2 substrate has also been demonstrated, with a tunable barrier height within a range of 0.24-0.91eV, potentially enabling current control over 10 orders of magnitude at room temperature. Through careful capacitance measurements, we show quantitatively that incomplete screening of an electric field from the degenerately doped Si back-gate through the MoS_2, leads to modulation of the Schottky barrier height at the graphene/MoS_2 interface through capacitive coupling to the

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gate. The optical response of the barristor is consistent with the changes in Schottky barrier height caused by the back-gate. The high photogain is attributed to the photoconductive gain that is likely present in the device. The barristor device is also used as a chemical/gas sensor with NO_2 and NH_3 being the test analyte species. It has been shown that the senstivity of the device can be effectively tuned by using the suitable gate-drain bias conditions, which allow the lower limit detections for these gases to go well below 1 ppm (close to 100 ppb for NO_2).

Finally, as a continuation of the present study on graphene-based barristors, a mixed dimensional barristor made of graphene/InN nanowire heterojunction with a backgate is demonstrated. The surface passivation of InN and the tunnel barrier formation at the graphene/NW interface were achieved through controlled O_2 plasma exposure, which allowed an otherwise ohmic contact to turn into a gate tunable Schottky junction with >1 eV barrier height. This device has been demostrated to perform sub-ppb level trace gas detection, photo-detection with very high sensitivity and a novel gate-controllable memristive action through longer O_2 plasma exposure.

7.2 Suggested Future Works

7.2.1 Transfer of MoS_2

Although our transfer-free growth has produced MoS_2 thin films with qualities comparable to the ones obtained from natural crystals, there are many substrates on which this method will not be suitable. For instance, polymeric substrates cannot withstand the temperature required for the growth. Also, if we want to make a MoS_2/graphene heterojunction with MoS_2 on top of graphene, this will also not be possible in the current method, as the O_2 used during the first step of the growth would

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have destroyed graphene. For such cases, it is important to find a way to transfer MoS_2 to a different substrate and minimize the damage to the film during this process.

Based on our preliminary works, we suggest a process flow for this purpose. At the beginning, the MoS_2 film has to be coated with PMMA or any suitable polymer. Then there are two possible ways to detach the film from SiO_2: one involves etching the SiO_2 using HF solution, the other involves using a intercalant such as HCl + H_2O_2. This intercalant seeps between MoS_2 and SiO_2 surfaces and gives off oxygen bubbles that separate the film supported by PMMA. The recipe should be tuned in a way so that there is enough force to lift the entire film off, but not too much of it to tear the film apart.

7.2.2 **MoS_2 Growth on Alternative Substrates**

Growing MoS_2 on other substrates will have immediate applications – MoS_2 on a flexible substrate would allow piezoresistive property of MoS_2 to be utilized. Also growing MoS_2 on wide bandgap materials such as GaN or SiC could help in fabricating high power device due its good current handling capability. The existing growth recipe can be used as a starting point to grow MoS_2 on substrates such as Si, sapphire, SiC, etc and then the growth parameters can be tweaked to achieve better results.

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Appendix A

Device Fabrication

1. Metal Deposition (Mo, Ti/Au)

Step	***Description***	***Process Details***
1.1	Sample Clean	Sonicate sample in acetone and IPA for 5 minutes each Dry sample using nitrogen
1.2	Optical Lithography	Lift-off Resist: LOR 3A/ LOR 5A Spin: 5000 rpm for 30 sec Soft bake: 150 °C for 1 min Photoresist: NR71-3000P Spin: 4000 rpm for 30 sec Pre-exposure bake: 150 °C for 1 min Exposure dose: 280 mJ/cm^2 Post-exposure bake: 100 °C for 1 min Developer: RD-6
1.3	Metal Deposition	Equipment: E-beam (or thermal) evaporator Pressure: below $2x10^{-6}$ Torr
1.4	Lift-off	Resist remover RR41 or 1165 Rinse with warm acetone and IPA

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2. GRAPHENE ETCH

Step	***Description***	***Process Details***
2.1	Sample Clean	Sonicate sample in acetone and IPA for 5 minutes each Dry sample using nitrogen
2.2	Optical Lithography	Lift-off Resist: LOR 3A/ LOR 5A Spin: 5000 rpm for 30 sec Soft bake: 150 °C for 1 min Photoresist: AZ1518 Spin: 5000 rpm for 30 sec Pre-exposure bake: 110 °C for 90 s Exposure dose: 150 mJ/cm^2 Developer: AZ400K : DI water (1:4) for ~60 sec
2.3	Plasma Etch	O_2 plasma for 3 min Pressure:300 mtorr Power: 150 W
2.4	Resist removal	Resist remover RR41 or 1165 Rinse with warm acetone and IPA

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